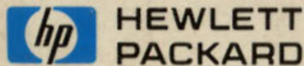
Hewlett-Packard Diode and Transistor Designer's Catalog 1982-83

Diode and Transistor Designer's Catalog 1982-83

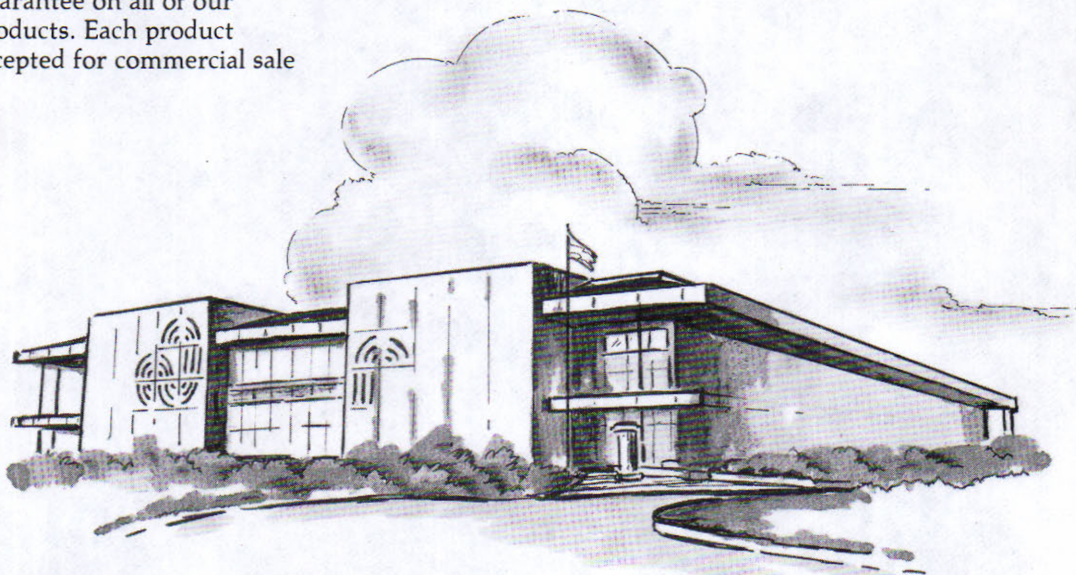


Microwave Semiconductor Diode and Transistor Designer's Catalog 1982-83

Intensive research, development of advanced manufacturing techniques and continued expansion has enabled Hewlett-Packard to become a high volume supplier of quality, competitively priced RF/Microwave Diodes and Transistors.

In addition to our broad product line, Hewlett-Packard also offers the following services: Applications support, special testing for customer requirements and a one year guarantee on all of our products. Each product accepted for commercial sale has been tested for reliability during the development phase and is subject to quality assurance procedures throughout the manufacturing process.

This package of products and services has enabled Hewlett-Packard to become a recognized leader in the Semiconductor Industry.



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Identifies newly introduced products or capabilities.
New products are also indicated by boldface listings in the Numeric Index.

A Brief Sketch

Hewlett-Packard, one of the world's leading designers and manufacturers of electronic, medical, analytical, and computing instruments and systems, diodes, transistors, integrated products, and optoelectronic products. Since its founding in Palo Alto, California, in 1939, HP has done its best to offer only products that represent significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue. This level of commitment enables the company to employ the latest technologies in developing innovative products that can be reliably produced, delivered, and supported on a continuing basis.

HP produces more than 3,500 products at our domestic divisions in California, Colorado, Washington, Oregon, Idaho, Massachusetts, New Jersey and Pennsylvania and at overseas plants located in the German Federal Republic, Scotland, France, Japan, Singapore, Malaysia and Brazil.

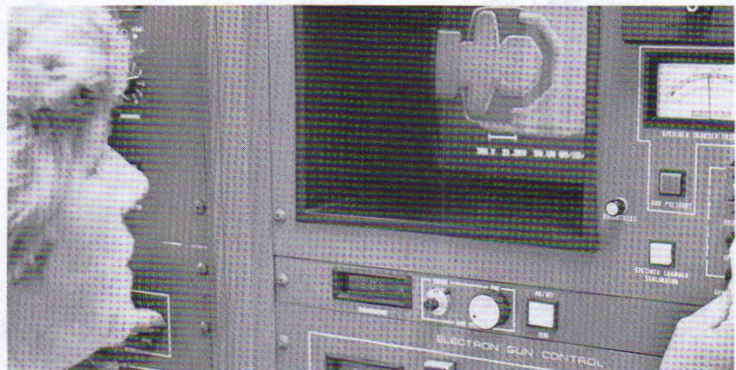
However, for the customer, Hewlett-Packard is no further away than the nearest telephone. Hewlett-Packard currently has sales and service offices located around the world. (Page 250) These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers.

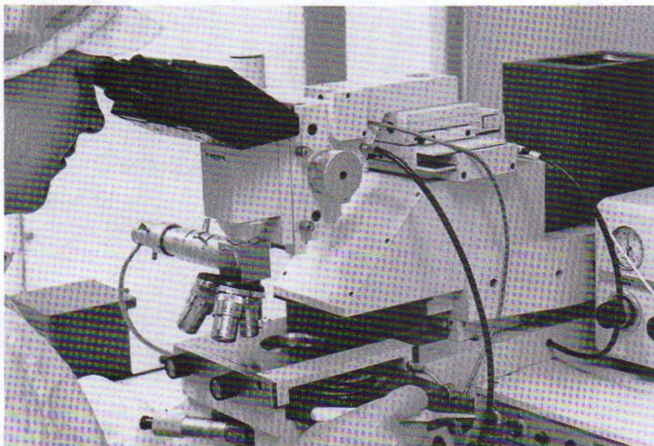
A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

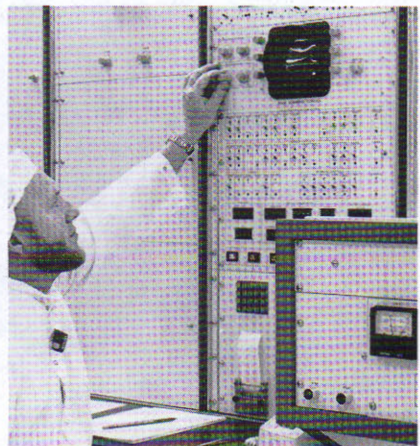
RF and Microwave Semiconductors

Hewlett-Packard has invested in a new 180,000 square foot manufacturing plant in San Jose, California. It houses modern equipment such as a computer controlled wafer fabrication facility which includes projection mask aligning and automation handling systems. Ion implantation, new evaporation and wet processing systems, and scanning electron microscopy provide the basis for quality and dependability for the entire product line.

When quality represents a competitive edge, or when reputation and dependability of your products is on the line, you can count on Hewlett-Packard RF and Microwave Semiconductor Devices for excellent product consistency.







About This Catalog

This Microwave Semiconductor Devices Designer's Catalog contains detailed and up-to-date specifications of our complete line of RF and microwave products. The catalog is divided into 7 product sections: Gallium Arsenide Field Effect Effect Transistors, Silicon Bipolar Transistors, Schottky Barrier Diodes, PIN and High Conductance Diodes, Step Recovery Diodes, Devices for Hybrid Integrated Circuits, and High Reliability Devices. At the end of each section, a selection of application notes pertaining to the use of those products is included.

Also included in each section where possible are the equivalent circuits of each product. These will be of use in the computer-aided design circuits.

In all of the transistor product data sheets, two tables for maximum ratings are shown. Recommended Maximum Continuous Operating Conditions indicate the conditions within which the device should be operated in order to meet the MTTF design goals for the device. The Absolute Maximum Ratings table indicates the limits of the device. Operation in excess of any of these conditions may result in permanent damage to the device. Package outlines are listed on page 238.

This catalog also provides a complete index of microwave semiconductor application notes on page 242.

How To Use This Catalog

Three methods are incorporated for locating components:

- A table of contents that allows you to locate devices by their general description.
- An alphanumeric index that lists all devices by part number plus generic chip part numbers.
- Selection guides at the beginning of each product section generally grouping products by major specification, frequency, etc.

Although product information and illustrations in these catalogs were current at the time it was approved for printing, Hewlett-Packard, in a continuing effort to offer excellent products at a fair value, reserves the right to change specifications, designs, and models without notice.

Ordering Information, After Sales Services

How To Order

All Hewlett-Packard components may be ordered through any of the Sales and Service offices listed on page 250. In addition, for immediate off-the-shelf delivery of Hewlett-Packard RF and Microwave Semiconductor devices, contact any of the worldwide stocking distributors and representatives listed on page 247.

Warranty

As an expression of confidence in our products to continue meeting the high standards of reliability and performance that customers have come to expect, Hewlett-Packard Microwave Semiconductor Products carry the following warranty.

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. HP will repair or, at its option, replace Components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

No other warranties are expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

EXCLUSIVE REMEDIES

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract tort or any other legal theory.

Certification

Some customers are especially interested in the test and quality assurance programs that HP applies to its products. These Hewlett-Packard programs are documented in a Certificate of Conformance which is available upon request at the time of purchase. This certification states:

We certify that the Microwave Semiconductor Division devices listed below were duly tested and inspected prior to shipment and that they met all of the published specifications for these devices.

Hewlett-Packard's calibration measurements are traceable to the National Bureau of Standards to the extent allowed by the Bureau's calibration facilities.

The Hewlett-Packard Quality Program satisfies the requirements of MIL-Q-9858A, MIL-I-45208A, MIL-C-45662A, and NASA 5300.4 (I.C.)

Service

We firmly believe that our obligation to you as a customer goes much beyond just the delivery of your new HP product. This philosophy is implemented by Hewlett-Packard in two basic ways: (1) by designing and building excellent products with good serviceability, and (2) by backing up those products with a customer service program which can respond to your needs with speed and completeness.

The HP customer service program is one of the most important facets of our worldwide operations, providing a local service capability in many of our field offices (listed on page 250). Indeed, this customer service program is one of the major factors in Hewlett-Packard's reputation for integrity and responsibility towards its customers.

Alphanumeric Index

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MODEL NO.	DESCRIPTION	GENERIC CHIP	PAGE NO.
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5082-2830	Monolithic Matched Schottky Diode Ring Quad	5082-9696	99

MODEL NO.	DESCRIPTION	GENERIC CHIP	PAGE NO.
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5082-3201	RF PIN Diode	5082-0012	142
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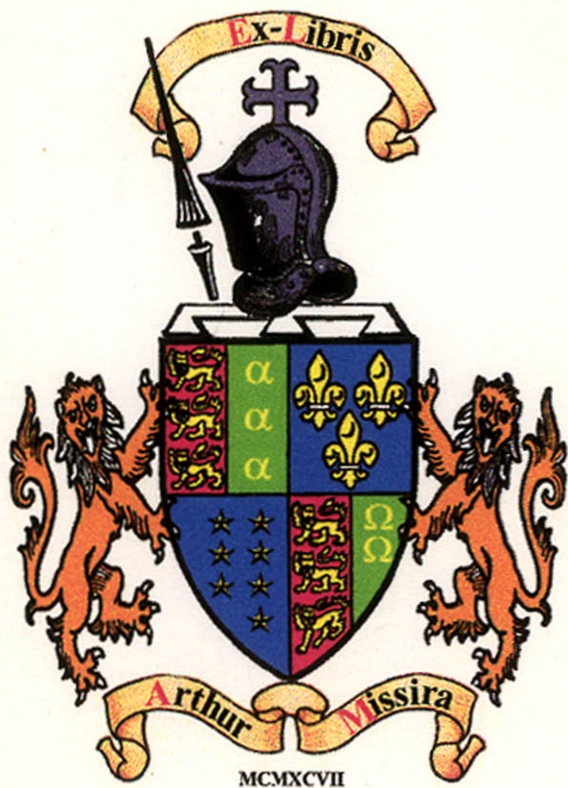
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Microwave GaAs FETs

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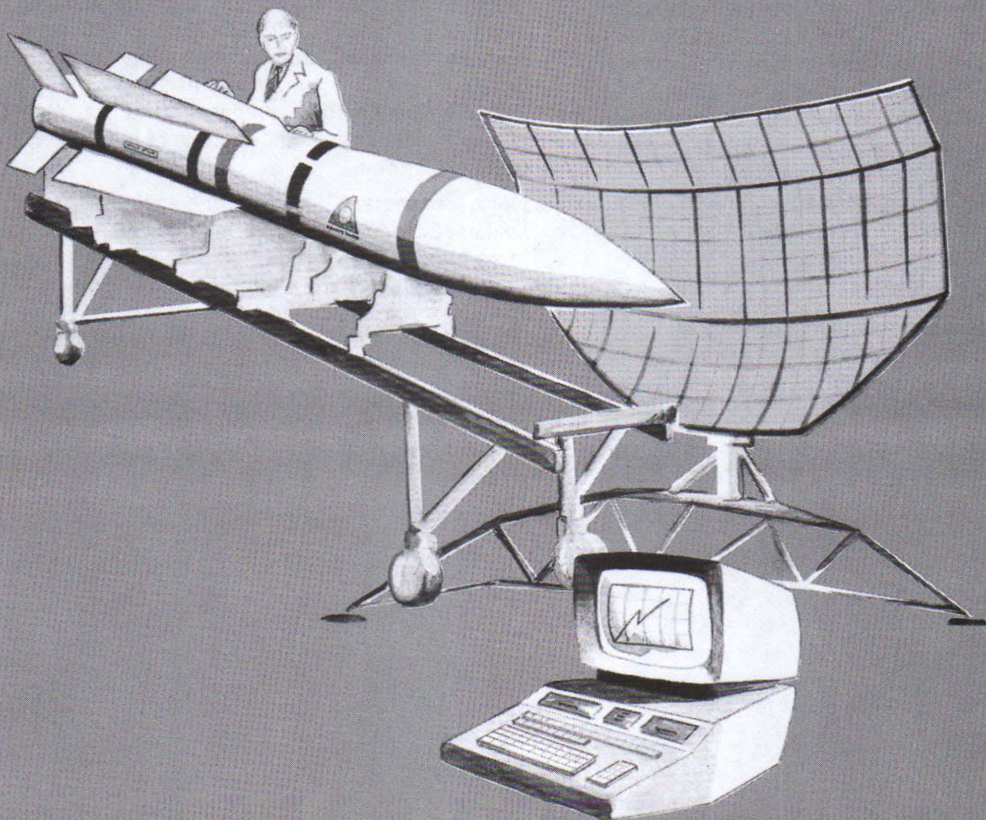


GaAs FET

Introduction

The gallium arsenide field effect transistor (GaAs FET), as the name implies, works by the field effect principle. A voltage (electric field) at the gate controls the flow of majority carriers (current) from drain to source in the gallium arsenide semiconducting material. Compared with the microwave silicon bipolar transistor, the GaAs FET has higher gain and lower noise figure, and can operate at a higher maximum frequency. The higher velocity of the majority carriers in the GaAs FET, compared with the slower minority carriers in the silicon bipolar transistor, is mainly responsible for the higher overall performance.

Applications

The GaAs FETs are most often used in amplifiers from below 1 GHz to beyond 18 GHz. They are also used in microwave oscillators and mixers.

DC Characteristics

The characteristics of the GaAs FETs can be measured by DC and RF means. The DC measurements are relatively easy to perform. Since each GaAs FET type has a characteristic DC behavior, DC measurements are used as a quality check in such areas as manufacturing and incoming inspection. The commonly measured DC parameters are saturated drain current (I_{DSS}), pinch off voltage (V_{GSP}) and transconductance (gm).

RF Characteristics

The RF measurements reveal directly the performance of the GaAs FETs in the RF frequency range. Each RF parameter is described briefly below.

Maximum available gain ($Ga_{(max)}$) is obtained by simultaneous conjugate match of the FET at its input and output. To obtain the high gain the FET is usually biased to a drain current of 100% I_{DSS}.

Minimum noise figure (F_{min}) and associated gain (Ga) are obtained when the input of the FET is tuned for the lowest noise figure and the output of the FET is tuned for maximum gain. For this test, the FET is usually biased to a current of 15% I_{DSS}.

Power at 1 dB compression (P_{1dB}) is the output of the FET when its input is increased sufficiently to produce a 1 dB drop in gain compared to the small signal gain. This test is usually performed with the FET drain current biased to 50% I_{DSS}.

S-parameters[1] are sets of four vectors (S_{11}, S_{21}, S_{12}, S_{22}) which describe the input impedance (S_{11}), output impedance (S_{22}), forward transmission (S_{21}) and reverse isolation (S_{12}) characteristics of the FET. They are tabulated for the intended operation frequency range of FET under various DC bias conditions such as low noise, high gain and linear power. Some of their uses are: impedance and gain calculations of the FET amplifier circuits and negative resistance computations of the FET oscillator circuits.

Noise parameters[1] contain one vector and two scalars. Source reflection coefficient (Γ_o) is the impedance that the FET should be presented at its input to result in a minimum noise figure (F_{min}) performance. The noise resistance (R_N) is a relative measure of how much noise figure degrades from its minimum value if the source impedance is changed from Γ_o. When Γ_o, F_{min} and R_N are known, noise figure trade off with gain can be calculated and plotted as noise circles.

Note 1: Hewlett-Packard Application Note AN154 — S-Parameter Design.

GaAs Field Effect Transistor Selection Guide

Part Number HFET-	Chip* Equivalent HFET-	Typical Noise Figure	Typical Associated Gain	Typical P_{1dB}	Frequency	Package HPAC-	Page Number
(2N6680) 1101	1001	1.6 dB	11 dB	+15.5 dBm	4 GHz	100A	4
1102	1001	1.4 dB	12 dB	+15.5 dBm	4 GHz	100A	4
2201	2001	2.4 dB	9.2 dB	+12.0 dBm	10 GHz	170	7
2202	2001	1.1 dB	13.6 dB	+15.5 dBm	4 GHz	100A	10
2204	2001	1.0 dB	13.6 dB	+15.5 dBm	4 GHz	100A	10

*For GaAs FET chip information see "Hybrid Integrated Circuits" section.

HEWLETT PACKARD

MICROWAVE GaAs FETS

2N6680 (HFET-1101) HFET-1102

Features

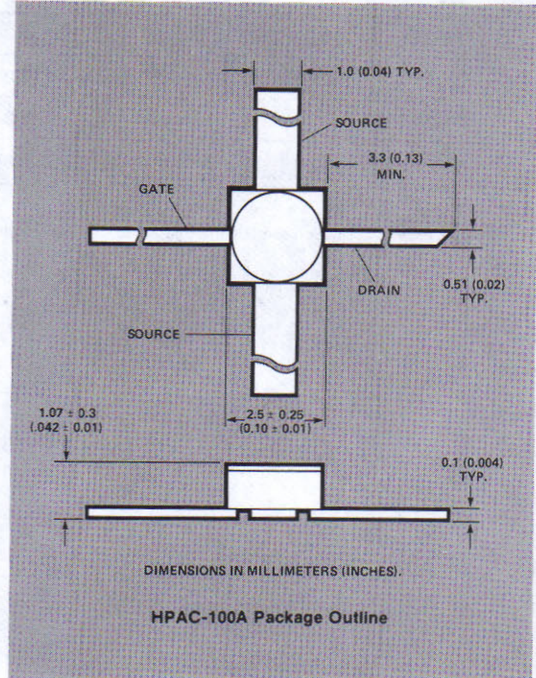
LOW NOISE FIGURE
- **1.6 dB Typical at 4 GHz (2N6680)**
- **1.7 dB Maximum at 4 GHz (HFET-1102)**
- **1.4 dB Typical**

HIGH GAIN
- **16 dB Typical at 4 GHz**

HIGH OUTPUT POWER
- **15.5 dBm Typical Linear Power Output at 4 GHz**

USABLE TO 12 GHz

RUGGED HERMETIC PACKAGE



HPAC-100A Package Outline

Description/Applications

The 2N6680 (HFET-1101) and the HFET-1102 are gallium arsenide Schottky gate field effect transistors in a package suitable for operation to 12 GHz. Their superior microwave performance in noise figure and gain make them useful for applications such as land and satellite communications, and radar.

2N6680 (HFET-1101) and HFET-1102 are supplied in the HPAC-100A, a rugged metal/ceramic hermetic package, and are capable of meeting the requirements of MIL-S-19500.

The HFET-1102 is a low noise and gain selection of the 2N6680.

High Reliability tested versions of both devices are also available.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 4.0V$, $V_{GS} = 0V$		mA	40		120
V_{GSP}	Pinch Off Voltage, $V_{DS} = 4.0V$, $I_{DS} < 100\ \mu A$		V	-1.5		-5.0
g_m	Transconductance, $V_{DS} = 4.0V$, $\Delta V_{GS} = 0V$ to $-0.5V$		mmho	30	40	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 4.0V$, $V_{GS} = 0$	f = 4 GHz	dB		16	
F_{MIN}	Noise Figure 2N6680: HFET-1102:	 f = 4 GHz 4 GHz	dB		 1.6 1.4	 2.2 1.7
G_a	Associated Gain 2N6680: HFET-1102: $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$ (Typ. 12 mA)	 f = 4 GHz 4 GHz	dB	 9.5 11.0	 11.0 12.0	
P_{1dB}	Power at 1 dB Compression, $V_{DS} = 5.0V$, $I_{DS} = 50\%\ I_{DSS}$ Tuned for Maximum Output Power at +5 dBm Input	f = 4 GHz 8 GHz	dBm		15.5 14.0	

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage -5.0V ≤ V_{GS} ≤ 0.0V	5V
V_{GS}[2]	Gate to Source Voltage 5.0V ≥ V_{DS} ≥ 0.0V	-5V
T_{CH}[3]	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3×10^6 hours at T_{CH} = 125°C (based on Activation Energy = 1.2 eV).
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. Θ_{jc} — Thermal resistance, channel to case = 200°C/W.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage -10V ≤ V_{GS} ≤ 0.0V	11V
V_{GS}[2]	Gate to Source Voltage 10.0V ≥ V_{DS} ≥ 0.0V	-10V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
Lead Soldering Temperature[3] 250°C for 10 sec. each lead.		

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward Gate Current should not exceed 3 mA.
3. See Handling and Use Precautions. (page 13).

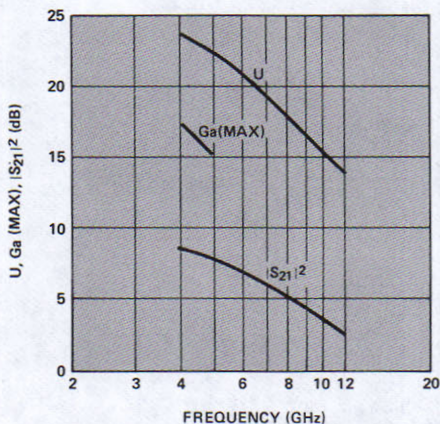


Figure 1. Typical Mason's Gain (U), $G_{a\,(max)}$, and $|S_{21}|^2$ vs. Frequency at V_{DS} = 4.0V, I_{DS} = 100% I_{DSS}.

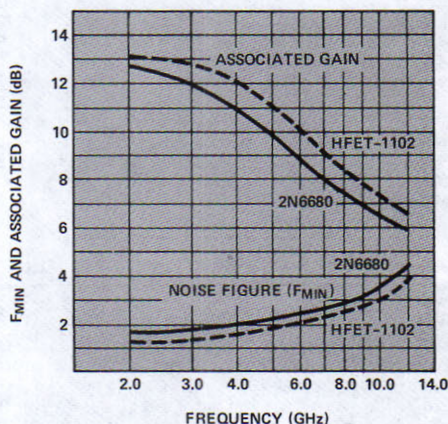


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency. V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

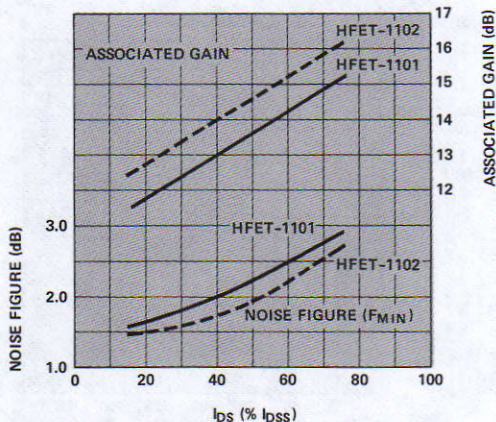


Figure 3. Typical Noise Figure and Associated Gain vs. Drain Current (I_{DS}) at 4 GHz, V_{DS} = 3.5V.

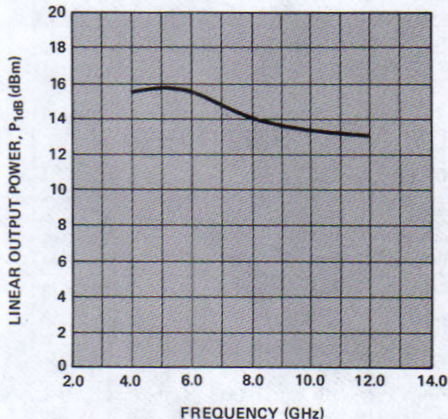


Figure 4. Typical Output Power at 1 dB Compression vs. Frequency. V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}. Tuned for Maximum Output Power at +5 dBm Input.

Typical S-Parameters

High Gain Bias: V_{DS} = 4.0V, V_{GS} = 0V

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.894	-60.6	3.122	123.6	.020	62.4	.781	-27.6
3.0	.801	-88.9	2.863	98.9	.025	55.8	.755	-40.5
4.0	.720	-116.2	2.597	75.6	.028	56.7	.732	-54.0
5.0	.662	-142.2	2.391	53.8	.034	62.0	.723	-67.7
6.0	.614	-167.4	2.187	32.4	.046	65.0	.716	-83.0
7.0	.588	169.3	1.985	12.1	.061	61.6	.711	-100.1
8.0	.580	148.1	1.807	-7.2	.083	54.8	.708	-118.2
9.0	.585	128.9	1.650	-25.6	.103	40.4	.720	-136.5
10.0	.593	110.9	1.535	-43.9	.121	31.1	.744	-155.5
11.0	.589	94.0	1.433	-62.6	.145	17.9	.765	-174.3
12.0	.574	76.6	1.329	-81.9	.164	2.4	.779	167.0

Linear Power Bias: V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.912	-57.8	2.836	125.2	.033	56.3	.705	-29.2
3.0	.829	-87.2	2.668	99.7	.044	41.7	.662	-43.7
4.0	.750	-116.5	2.458	74.5	.050	30.2	.632	-59.3
5.0	.683	-144.1	2.259	51.1	.054	21.5	.610	-76.3
6.0	.641	-171.3	2.053	28.5	.057	16.3	.572	-95.7
7.0	.625	164.1	1.847	6.3	.061	13.6	.556	-115.1
8.0	.621	142.7	1.664	-14.0	.069	9.8	.554	-133.0
9.0	.626	124.9	1.510	-33.1	.080	3.5	.589	-155.0
10.0	.627	108.4	1.382	-51.3	.095	-3.7	.609	-175.8
11.0	.615	92.4	1.257	-70.1	.106	-14.4	.614	166.3
12.0	.598	76.6	1.155	-88.0	.123	-26.1	.624	150.6

Minimum Noise Figure Bias: V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.935	-51.9	2.166	128.3	.045	54.6	.733	-30.5
3.0	.862	-77.1	2.070	104.4	.060	39.3	.697	-45.4
4.0	.792	-102.4	1.955	81.1	.070	26.0	.659	-60.8
5.0	.733	-127.2	1.860	58.7	.074	14.8	.630	-76.0
6.0	.674	-152.0	1.740	36.4	.075	6.2	.600	-92.6
7.0	.631	-175.5	1.599	15.2	.074	1.3	.578	-110.8
8.0	.607	162.8	1.469	-4.4	.077	.5	.565	-129.5
9.0	.601	143.0	1.352	-23.4	.087	-6.2	.570	-148.4
10.0	.602	124.5	1.261	-41.8	.091	-10.3	.585	-167.6
11.0	.594	107.3	1.180	-60.5	.104	-16.4	.600	173.5
12.0	.575	90.0	1.101	-79.5	.119	-27.0	.613	154.6

Typical Noise Parameters[1]

2N6680 (HFET-1101)

Frequency (GHz)	Γ_o		F_{MIN} (dB)	R_N (Ohms)
	Mag.	Ang.		
2.0	.730	60°	1.25	19.40
4.0	.618	98°	1.60	23.14
6.0	.575	138°	2.20	6.64
8.0	.617	-170°	2.80	1.88
10.0	.610	-128°	3.60	25.47
12.0	.660	-87°	4.50	49.10

Note:

1. Optimum source reflection coefficient for minimum noise figure (Γ_o), Minimum Noise Figure (F_{min}) and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.
   Optimum match points for HFET-1102 are equivalent.

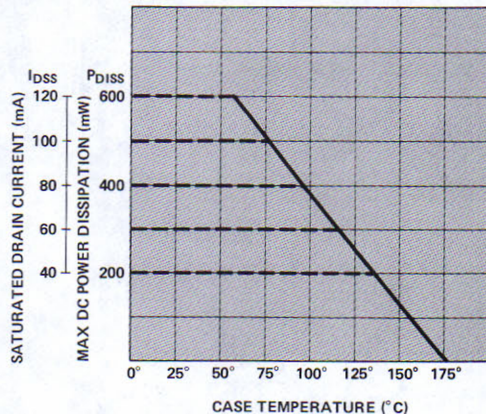


Figure 5. PDISS vs. Temperature, Power Derating Curve at V_{DS} = 5V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with solid diagonal line.

HEWLETT PACKARD

LOW NOISE BROADBAND MICROWAVE GaAs FET

HFET-2201

Features

LOW NOISE FIGURE
2.4 dB Typical NF at 10 GHz
3.1 dB Typical NF at 14 GHz

HIGH MAXIMUM AVAILABLE GAIN
14.5 dB Typical $G_{a(max)}$ at 10 GHz

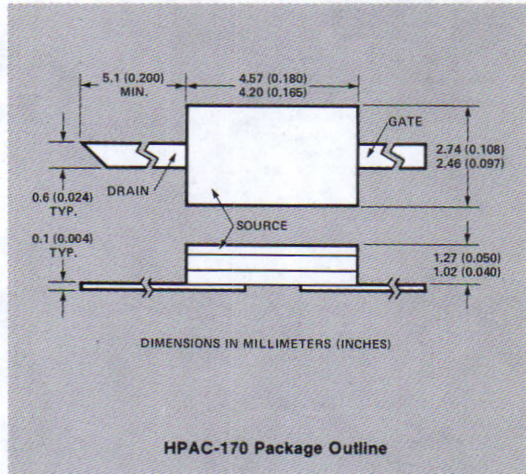
HIGH OUTPUT POWER
12 dBm Linear Power at 10 GHz

CHARACTERIZED TO 18 GHz

HERMETIC MICROSTRIP WIDEBAND PACKAGE

HIGH TRANSDUCER GAIN TO 18 GHz

0.5 MICROMETER GATE



HPAC-170 Package Outline

Description/Applications

The HFET-2201 is a gallium arsenide Schottky gate field effect transistor. It features a rugged, hermetic, microstrip compatible package that is designed for consistent broadband or narrow-band operation over the frequency range of 2 GHz to 18 GHz. The device's superior noise and gain performance, coupled with its wide dynamic range capability make it ideally suited for such applications as ECM, wideband surveillance, and warning systems.

In addition, its characteristics lend themselves to ease of circuit design in applications such as radar and communications equipment.

The HFET-2201 is packaged in the HPAC-170. The part is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

High Reliability tested versions of this device are also available.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 3.5V$, $V_{GS} = 0V$		mA	25	45	90
V_{GSP}	Pinch Off Voltage, $V_{DS} = 3.5V$, $I_{DS} < 500\mu A$		V	-0.5	-2.0	-4.0
g_m	Transconductance, $V_{DS} = 3.5V$, $\Delta V_{GS} = 0V$ to $-0.5V$		mmho	20	32	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 3.5V$, $V_{GS} = 0V$	f= 8GHz	dB		16.0	
		10GHz	dB		14.5	
		12GHz	dB		12.5	
F_{MIN}	Minimum Noise Figure $V_{DS} = 3.5V$, $I_{DS} = 15\%$ I_{DSS} (Typ. 7.5mA)	f= 4GHz	dB		1.2	
		10GHz	dB		2.4	2.8
		14GHz	dB		3.1	
G_a	Associated Gain At N.F. Bias	f= 4GHz	dB		14.1	
		10GHz	dB	8.0	9.2	
		14GHz	dB		8.0	
P_{1dB}	Power at 1dB Compression $V_{DS} = 3.5V$, $I_{DS} = 50\%$ I_{DSS} (0 dBm Input Matching, Tuned for Max. Output)	f=10GHz	dBm		12.0	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-4.0V \leq V_{GS} \leq 0.0V$	4V
V_{GS}[2]	Gate to Source Voltage $4.0V \geq V_{DS} \geq 0.0V$	-4V
T_{CH}[3]	Maximum Channel Temperature	125°C
T_{STG}	Storage Temperature	-65°C to +125°C

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3 x 10^6 hours at T_{CH} = 125°C (based on Activation Energy = 1.2 eV).
2. Maximum Continuous Forward Gate Current should not exceed 1.5 mA.
3. θ_{jc} — Thermal resistance, channel to case = 230°C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-4V \leq V_{GS} \leq 0.0V$	10V
V_{GS}[2]	Gate to Source Voltage $4V \geq V_{DS} \geq 0.0V$	-6V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
LID and Lead Soldering Temp.[3] 250°C for 10 sec. each item.		

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward Gate Current should not exceed 2 mA.
3. See Handling and Use Precautions. (page 13).

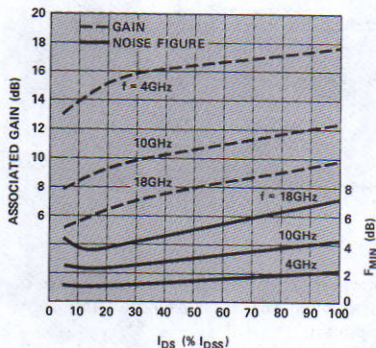


Figure 1. Typical Associated Gain and Noise Figure (F_{min}) vs. I_{DS} as a percentage of I_{DSS} when tuned for minimum noise figure. Frequency from 4 GHz to 18 GHz, V_{DS} = 3.5V.

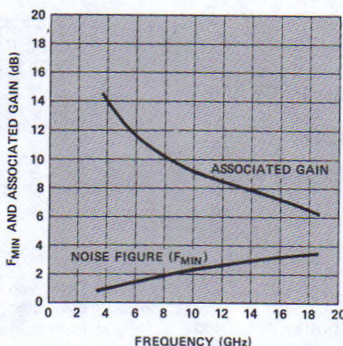


Figure 2. Typical Noise Figure (F_{min}) and Associated Gain vs. Frequency, V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

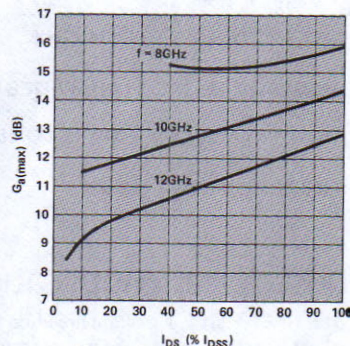


Figure 3. Typical $G_{a(max)}$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 8, 10, and 12 GHz, V_{DS} = 3.5V.

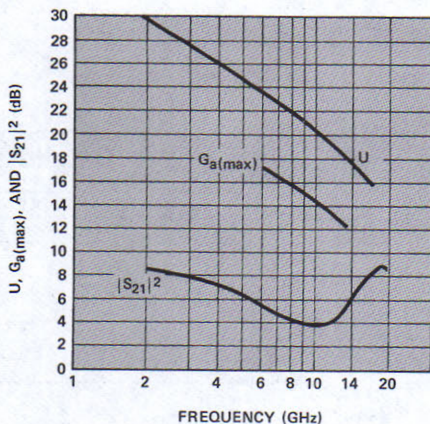


Figure 4. Mason's Gain (U), $G_{a(max)}$ and $|S_{21}|^2$ vs. Frequency. V_{DS} = 3.5V, V_{GS} = 0.0V.

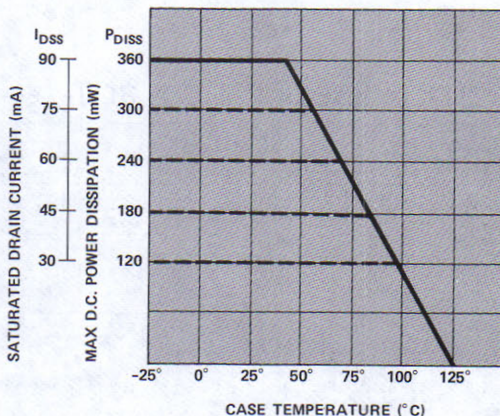


Figure 5. P_{DISS} vs. Temperature, Power Derating Curve at V_{DS} = 4V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with the solid diagonal line.

Typical S-Parameters Minimum Noise Figure Bias V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang
2.00	0.98	-58	5.67	1.92	127	-31.09	0.03	45	0.79	-34
3.00	0.96	-82	5.07	1.79	103	-28.37	0.04	26	0.77	-50
4.00	0.96	-106	4.52	1.68	81	-26.62	0.05	9	0.77	-66
5.00	0.92	-127	3.91	1.57	59	-25.76	0.05	-8	0.74	-82
6.00	0.91	-146	3.28	1.46	39	-25.39	0.05	-24	0.71	-97
7.00	0.90	-164	2.72	1.37	19	-24.99	0.06	-37	0.69	-113
8.00	0.89	-178	2.23	1.29	0	-24.81	0.06	-49	0.68	-130
9.00	0.88	170	1.82	1.23	-17	-24.62	0.06	-62	0.67	-147
10.00	0.87	159	1.68	1.21	-34	-24.28	0.06	-74	0.66	-162
11.00	0.86	148	1.80	1.23	-51	-24.17	0.06	-84	0.62	-175
12.00	0.84	138	2.25	1.30	-68	-23.37	0.07	-93	0.57	174
13.00	0.81	125	3.01	1.41	-88	-21.70	0.08	-106	0.49	161
14.00	0.77	108	4.04	1.59	-111	-20.34	0.10	-125	0.36	144
15.00	0.70	87	4.77	1.73	-138	-19.12	0.11	-147	0.17	120
16.00	0.60	61	5.24	1.83	-169	-18.28	0.12	-169	0.08	-57
17.00	0.48	30	5.01	1.78	158	-17.29	0.14	162	0.35	-95
18.00	0.36	-8	3.99	1.58	124	-17.58	0.13	130	0.60	-124

Typical S-Parameters Maximum Gain Bias V_{DS} = 3.5V, I_{DS} = 100% I_{DSS}

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.00	0.97	-64	8.83	2.76	124	-35.40	0.02	44	0.80	-33
3.00	0.94	-91	8.03	2.52	99	-32.94	0.02	30	0.79	-49
4.00	0.93	-116	7.25	2.30	77	-31.57	0.03	14	0.79	-64
5.00	0.90	-137	6.48	2.11	56	-30.97	0.03	0	0.76	-79
6.00	0.88	-156	5.73	1.93	36	-30.99	0.03	-12	0.74	-95
7.00	0.86	-173	5.06	1.79	16	-30.69	0.03	-18	0.72	-110
8.00	0.85	173	4.50	1.68	-2	-30.29	0.03	-24	0.73	-126
9.00	0.84	161	4.03	1.59	-19	-30.15	0.03	-30	0.72	-143
10.00	0.83	151	3.90	1.57	-35	-28.93	0.04	-35	0.72	-158
11.00	0.80	140	3.98	1.58	-52	-28.16	0.04	-41	0.69	-170
12.00	0.78	129	4.39	1.66	-69	-26.36	0.05	-47	0.65	179
13.00	0.75	116	5.15	1.81	-88	-24.15	0.06	-57	0.61	168
14.00	0.72	99	6.29	2.06	-110	-21.76	0.08	-73	0.55	151
15.00	0.70	76	7.41	2.35	-135	-19.29	0.10	-95	0.43	125
16.00	0.67	45	8.39	2.63	-167	-17.50	0.13	-121	0.25	79
17.00	0.65	4	8.65	2.71	156	-15.79	0.16	-151	0.23	-23
18.00	0.62	-42	7.83	2.46	116	-14.78	0.18	169	0.55	-89

Typical Noise Parameters[1]

Frequency (GHz)	Γ_o		F_{MIN} (dB)	R_N (Ohms)
	Mag.	Ang.		
4.0	.847	92	1.12	47
6.0	.779	142	1.7	14
8.0	.789	168	2.0	2
10.0	.814	-172	2.4	8
12.0	.645	-153	2.7	30
14.0	.600	-114	3.1	4.3
18.0	.329	-36	3.4	—

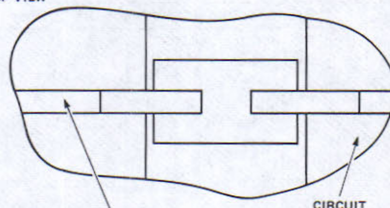
Note:

1. Optimum source reflection coefficient for minimum noise figure (Γ_o), Minimum Noise Figure (F_{min}) and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

Mounting Instructions

THE USE OF CONVENTIONAL LEAD-TIN SOLDER IS RECOMMENDED FOR PACKAGE MOUNTING. CARE SHOULD BE TAKEN TO INSURE GOOD SOLDER WETTING TO MINIMIZE SOURCE INDUCTANCE AND THERMAL RESISTANCE.

TOP VIEW



SIDE VIEW

For more information on mounting the HPAC-170 see Application Bulletin 24 (Publication Number 5952-9881).

HEWLETT PACKARD

LOW NOISE MICROWAVE GaAs FETS

HFET-2202 HFET-2204

Features

LOW NOISE FIGURE

HFET-2204:

1.0 dB Typical NF at 4 GHz, 1.1 dB Maximum
2.1 dB Typical NF at 10 GHz

HFET-2202:

1.1 dB Typical NF at 4 GHz, 1.4 dB Maximum
1.9 dB Typical NF at 8 GHz

HIGH ASSOCIATED GAIN

13.6 dB Typical G_a at 4 GHz, 12.0 dB Minimum

HIGH OUTPUT POWER

15.5 dBm Linear Power at 4 GHz

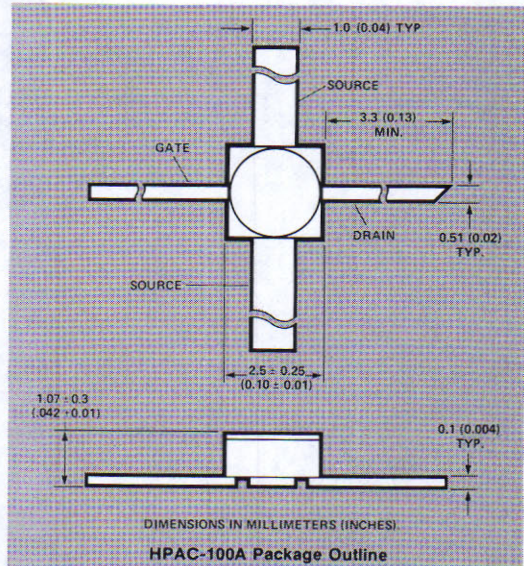
CHARACTERIZED TO 12 GHz

RUGGED HERMETIC PACKAGE

0.5 MICROMETER GATE

Description/Applications

The HFET-2202 and HFET-2204 are gallium arsenide Schottky gate field effect transistors that feature a rugged, hermetic package designed for consistent operation over the frequency range of 2 GHz to 12 GHz. The superior noise and gain performance of these devices, coupled with their wide dynamic range capability, make them ideally suited for such applications as land and satellite communications and radar.



HPAC-100A Package Outline

The HFET-2202 and HFET-2204 are packaged in the HPAC-100A. They are capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 3.5V$, $V_{GS} = 0V$	mA	25	45	90
V_{GSP}	Pinch Off Voltage, $V_{DS} = 3.5V$, $I_{DS} < 500\mu A$	V	-0.5	-2.0	-4.0
g_m	Transconductance, $V_{DS} = 3.5V$, $\Delta V_{GS} = 0V$ to $-0.5V$	mmho	20	32	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 3.5V$, $V_{GS} = 0V$ f = 6 GHz 8 GHz	dB		16.0 13.0	
F_{MIN}	Minimum Noise Figure **HFET-2204** $V_{DS} = 3.5V$, $I_{DS} = 15\%$ I_{DSS} (Typ. 7.5 mA) f = 4 GHz 6 GHz 8 GHz 10 GHz	dB		1.0 1.3 1.6 2.1	1.1
G_a	Associated Gain at N.F. Bias f = 4 GHz 6 GHz 8 GHz 10 GHz	dB	12.0	13.6 11.9 10.2 9.1	
F_{MIN}	Minimum Noise Figure **HFET-2202** $V_{DS} = 3.5V$, $I_{DS} = 15\%$ I_{DSS} (Typ. 7.5 mA) f = 4 GHz 6 GHz 8 GHz	dB		1.1 1.4 1.9	1.4
G_a	Associated Gain at N.F. Bias f = 4 GHz 6 GHz 8 GHz	dB	12.0	13.6 11.3 9.6	
P_{1dB}	Power at 1 dB Gain Compression f = 4 GHz	dBm		15.5	
G_{1dB}	Associated 1 dB Compressed Gain f = 4 GHz $V_{DS} = 4.0V$, $I_{DS} = 50\%$ I_{DSS} (0 dBm Input Matching, Tuned for Maximum Output)	dB		15.0	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage, $-4\ V \leq V_{GS} \leq 0V$	4V
V_{GS}[2]	Gate to Source Voltage $4V \geq V_{DS} \geq 0V$	-4V
T_{CH}[3]	Maximum Channel Temperature	125°C
T_{STG}	Storage Temperature	-65°C to +125°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3×10^6 hours at $T_{CH} = 125°C$ (based on Activation Energy = 1.2 eV).
2. Maximum Continuous Forward Gate Current should not exceed 1.5 mA.
3. Θ_{jc} — Thermal resistance, channel to case = 260° C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-4V \leq V_{GS} \leq 0V$	10V
V_{GS}[2]	Gate to Source Voltage $4V \geq V_{DS} \geq 0V$	-6V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(max)}$	Maximum Storage Temperature	250°C
Lead Soldering Temperature[3]: 250°C for 10 sec. each lead.		

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward gate current should not exceed 2 mA.
3. See Handling and Use Precautions (page 3).

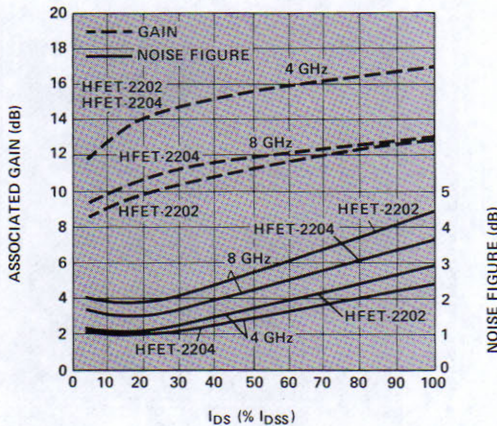


Figure 1. Typical Associated Gain and Noise Figure (F_{MIN}) vs. I_{DS} as a percentage of I_{DSS} when tuned for minimum noise figure at 4 GHz and 8 GHz, $V_{DS} = 3.5V$.

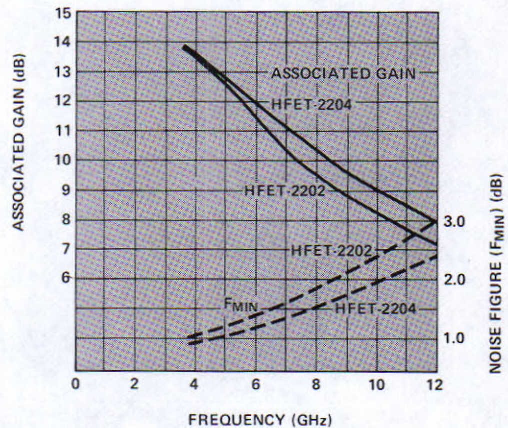


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency. $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$.

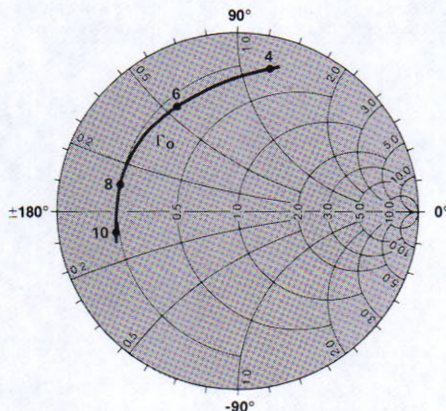


Figure 3. Typical Γ_o in the 4 to 10 GHz range for $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$. Γ_o = Input Match for Minimum Noise.

TABLE I. HFET-2204 Typical Noise Parameters[1]

Frequency	Γ_o	F_{MIN} (dB)	R_N (Ω)
4 GHz	.83 ∠ 78°	1.0	33
6 GHz	.68 ∠ 120°	1.3	14
8 GHz	.67 ∠ 167°	1.6	2
10 GHz	.68 ∠ -170°	2.1	3

1. Optimum source reflection coefficient for minimum noise figure (Γ_o), Minimum Noise Figure (F_{min}) and Noise Resistance (R_N) at $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$.
Optimum match points for HFET-2202 are equivalent.

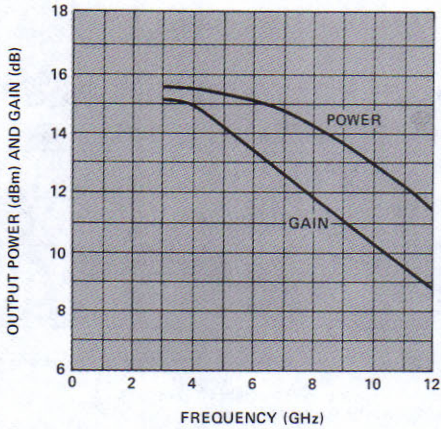


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}.

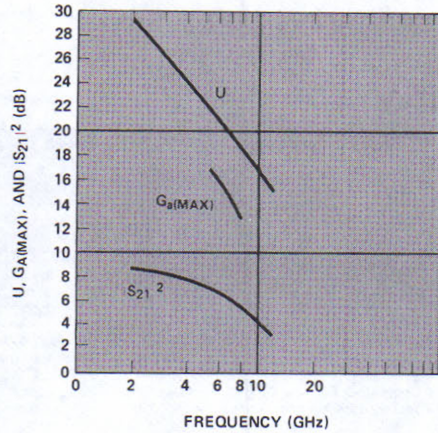


Figure 5. Typical Mason's Gain (U), $G_{a(max)}$ and $[S_{21}]^2$ vs. Frequency, V_{DS} = 3.5V, V_{GS} = 0.0V.

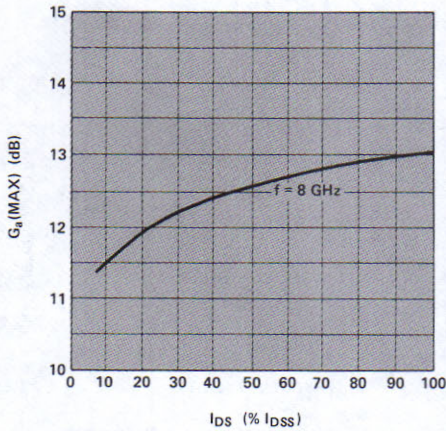


Figure 6. Typical $G_{a(max)}$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 8 GHz. V_{DS} = 3.5V.

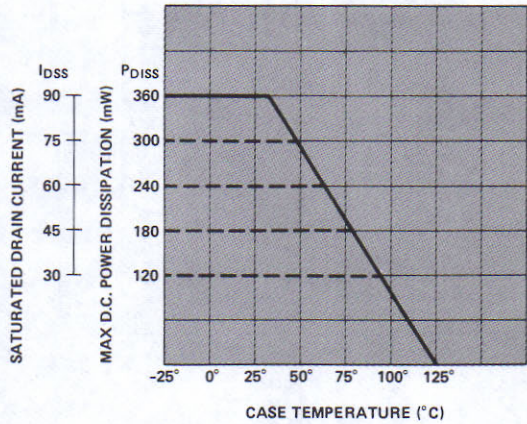


Figure 7. P_{DISS} vs. Temperature, Power Derating Curve at V_{DS} = 4V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with the solid diagonal line.

Typical S-Parameters

MINIMUM NOISE FIGURE BIAS V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.977	-41	5.56	1.897	141	-30.2	0.031	61	0.730	-26
3.0	0.952	-61	5.41	1.865	121	-27.3	0.043	46	0.714	-38
3.5	0.924	-71	5.39	1.860	112	-26.2	0.049	40	0.704	-45
3.6	0.923	-73	5.38	1.858	109	-26.0	0.050	39	0.702	-45
3.7	0.922	-76	5.36	1.853	107	-25.9	0.051	38	0.698	-47
3.8	0.922	-78	5.33	1.848	106	-25.7	0.052	37	0.692	-48
3.9	0.921	-80	5.32	1.846	103	-25.5	0.053	35	0.685	-50
4.0	0.920	-82	5.28	1.836	102	-25.4	0.054	34	0.684	-51
4.1	0.916	-83	5.24	1.828	100	-25.2	0.055	33	0.683	-52
4.2	0.914	-85	5.20	1.820	99	-25.0	0.056	32	0.683	-53
4.3	0.910	-87	5.19	1.818	96	-24.7	0.058	31	0.683	-54
4.4	0.900	-89	5.18	1.815	94	-24.9	0.057	28	0.682	-56
4.5	0.898	-91	5.17	1.813	93	-24.7	0.058	28	0.681	-57
5.0	0.883	-102	5.16	1.811	83	-24.2	0.062	21	0.667	-63
6.0	0.839	-124	4.88	1.753	63	-23.5	0.067	10	0.638	-76
7.0	0.805	-145	4.50	1.679	45	-23.4	0.068	-2	0.602	-90
8.0	0.777	-164	4.14	1.610	26	-23.4	0.068	-10	0.568	-106
9.0	0.759	178	3.67	1.526	8	-23.5	0.067	-16	0.541	-124
10.0	0.743	161	3.14	1.436	-9	-23.5	0.067	-21	0.531	-142
11.0	0.727	145	2.67	1.360	-26	-23.3	0.069	-24	0.528	-161
12.0	0.722	130	2.27	1.299	-43	-22.6	0.074	-27	0.537	-177

HIGH GAIN BIAS V_{DS} = 3.5V, V_{GS} = 0V

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.952	-47	9.15	2.868	137	-33.6	0.021	63	0.705	-25
3.0	0.911	-70	8.78	2.747	116	-30.8	0.029	51	0.688	-37
3.5	0.874	-81	8.55	2.677	106	-30.2	0.031	47	0.677	-43
3.6	0.871	-84	8.52	2.668	104	-29.9	0.032	45	0.675	-44
3.7	0.866	-86	8.52	2.666	101	-29.6	0.033	45	0.672	-45
3.8	0.865	-89	8.51	2.664	100	-29.6	0.033	44	0.666	-46
3.9	0.865	-91	8.46	2.650	97	-29.4	0.034	42	0.660	-47
4.0	0.861	-93	8.37	2.624	96	-29.4	0.034	42	0.660	-49
4.1	0.857	-94	8.38	2.625	94	-29.1	0.035	41	0.660	-50
4.2	0.855	-96	8.34	2.611	92	-29.1	0.035	41	0.660	-51
4.3	0.856	-99	8.30	2.601	90	-28.9	0.036	40	0.660	-52
4.4	0.835	-101	8.17	2.563	88	-28.9	0.036	39	0.660	-53
4.5	0.832	-103	8.11	2.545	87	-28.9	0.036	38	0.656	-54
5.0	0.814	-115	8.05	2.525	77	-28.2	0.039	35	0.645	-60
6.0	0.765	-138	7.48	2.367	57	-27.5	0.042	30	0.622	-72
7.0	0.732	-159	6.92	2.219	39	-26.7	0.046	26	0.594	-85
8.0	0.709	-179	6.37	2.082	20	-25.9	0.051	23	0.566	-100
9.0	0.697	164	5.80	1.950	3	-24.6	0.059	19	0.544	-117
10.0	0.690	147	5.23	1.825	-14	-23.2	0.069	15	0.541	-136
11.0	0.678	131	4.69	1.716	-30	-21.8	0.081	8	0.541	-154
12.0	0.673	117	4.24	1.629	-47	-20.7	0.092	-1	0.556	-171

LINEAR POWER BIAS V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.968	-44	8.07	2.532	139	-32.4	0.024	62	0.708	-25
3.0	0.933	-65	7.80	2.454	119	-29.6	0.033	49	0.691	-37
3.5	0.900	-76	7.63	2.408	109	-28.6	0.037	44	0.681	-43
3.6	0.898	-78	7.63	2.408	107	-28.4	0.038	43	0.679	-44
3.7	0.893	-81	7.63	2.408	104	-28.4	0.038	42	0.675	-45
3.8	0.889	-83	7.63	2.408	103	-28.2	0.039	41	0.670	-47
3.9	0.890	-85	7.60	2.399	101	-28.2	0.039	39	0.664	-48
4.0	0.890	-87	7.54	2.381	99	-28.0	0.040	39	0.663	-49
4.1	0.887	-88	7.52	2.378	97	-27.7	0.041	38	0.663	-50
4.2	0.885	-90	7.48	2.365	96	-27.7	0.041	37	0.663	-51
4.3	0.887	-93	7.43	2.351	93	-27.3	0.043	36	0.663	-52
4.4	0.867	-95	7.36	2.333	91	-27.5	0.042	34	0.663	-54
4.5	0.865	-97	7.32	2.323	90	-27.3	0.043	34	0.659	-55
5.0	0.847	-108	7.30	2.318	80	-26.7	0.046	29	0.648	-61
6.0	0.798	-131	6.86	2.203	60	-26.2	0.049	21	0.621	-73
7.0	0.762	-152	6.39	2.086	42	-25.9	0.051	14	0.589	-87
8.0	0.736	-171	5.89	1.970	23	-25.4	0.054	10	0.558	-102
9.0	0.720	171	5.38	1.857	6	-24.7	0.058	7	0.534	-119
10.0	0.707	154	4.82	1.741	-11	-23.9	0.064	3	0.527	-137
11.0	0.693	138	4.31	1.643	-28	-22.7	0.073	-2	0.528	-155
12.0	0.689	124	3.88	1.564	-44	-21.6	0.083	-8	0.541	-172

Handling And Use Precautions

The GaAs FETs are subject to damage caused by switching transients and static discharge, and must be handled with caution. Hewlett-Packard recommends the following precautions.

1. Assembly and test personnel, as well as tweezers or any other pick-up tool, should be grounded to the test or assembly station, preventing the build-up of static charge which can damage the gate area if the charge is allowed to pass through it. During the package mounting procedure, insure assembly equipment is adequately grounded.

   Static discharge during handling, testing, and assembly can induce increased reverse gate leakage of a resistive nature.

   To prevent the buildup of static charge on the package during storage, the device should be held in a conductive medium (e.g., metal container, conductive foam).

2. Spurious pulses generated by test equipment (i.e. contact bounce during switching, induced voltage in the leads, etc.) must be eliminated. Avoid turning instrument power on and off, or switching between instrument ranges when bias is applied to the device.

3. Inductive pickup from large transformers, switching power supplies, inductive ovens, etc., must also be eliminated. Use shielded signal and power cables.

4. Assembly equipment (e.g., soldering irons) must be adequately grounded.

5. Application of bias. When applying bias to the FET, first apply the gate voltage, then the drain voltage. When removing bias, remove the gate voltage last.

Applications for Microwave GaAs FETS

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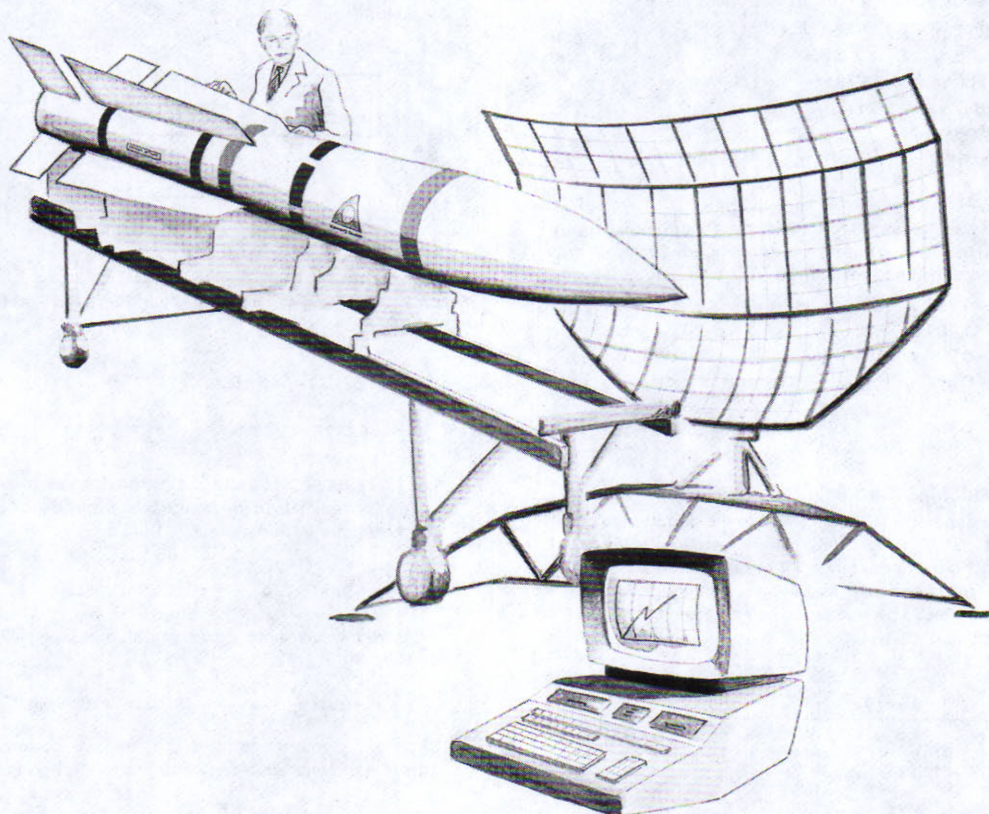


HEWLETT PACKARD

APPLICATIONS FOR MICROWAVE GaAs FETs

12 GHz Amplifier Designs Using the HFET-2201

(Portion of Application Note 973)

INTRODUCTION

This application note presents two single-ended amplifier designs from 11.7 to 12.2 GHz using the HFET-2201. The first design, a low noise amplifier, achieves a noise figure of 3.1 dB at 12 GHz with 7.5 dB of associated gain on an alumina substrate. The second design, a high gain stage, obtains greater than 11.5 dB of gain across the band on RT/Duroid.[1]

THE LOW NOISE DESIGN

This design explains in detail an 11.7 to 12.2 GHz low noise amplifier. Input and output matching networks are described. The construction, mounting and bias considerations are included.

The initial design goals are:

- Frequency Range = 11.7 to 12.2 GHz
- Amplifier Noise Figure ≤ 3.4 dB
- Associated Gain ≥ 7.0 dB
- Gain Flatness = ±.5 dB
- Output SWR ≤ 1.5:1
- Bias Conditions
  V_{DS} = 3.5V I_{DS} = 15% I_{DSS}

Design Data

A device was measured for S-parameters and noise figure at 12 GHz. The optimum source impedance (Γ_o) was measured and noise resistance (R_N) was calculated.

S_{11}	= 0.795 ∠ 137°	Γ_{MS}	= .858 ∠ -131°
S_{21}	= 1.307 ∠ -67°	Γ_{ML}	= .703 ∠ -148°
S_{12}	= 0.077 ∠ -80°	F_{min}	= 2.8 dB
S_{22}	= 0.582 ∠ 169°	G_a	= 8.2 dB
K	= 1.28	Γ_o	= .73 ∠-141°
Ga_{max}	= 9.1 dB	Γ_L	= .570 ∠ -152°
		R_N	= 18Ω

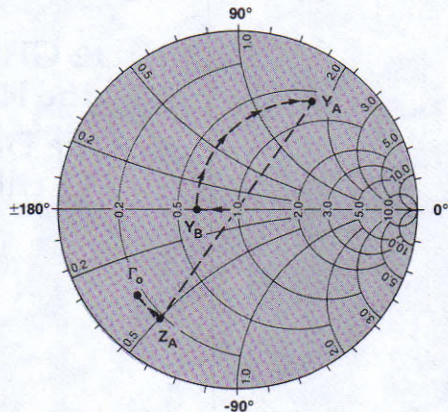
Input Matching Circuit

The 50Ω generator is transformed to the admittance corresponding to Γ_o using Smith Chart techniques (Figure 1). Bonding ribbon inductance must be accounted for in the design. This is done by, assuming a bonding inductance of 0.1 nH, subtracting a reactance of 7.5Ω from the impedance corresponding to Γ_o.

$$X_L = \omega L = 2\pi\,(12\text{ GHz})\,(0.1\text{ nH}) = 7.5\Omega$$

$$Z_{NF} = \frac{(1 - |\Gamma_o|^2)\,50}{1 + |\Gamma_o|^2 - 2\,|\Gamma_o|\cos\angle\Gamma_o} + j\,\frac{(2\,|\Gamma_o|\sin\angle\Gamma_o)\,50}{1 + |\Gamma_o|^2 - 2\,|\Gamma_o|\cos\angle\Gamma_o}$$

$$Z_{NF} = 8.76 - j\,17.22\ \Omega$$



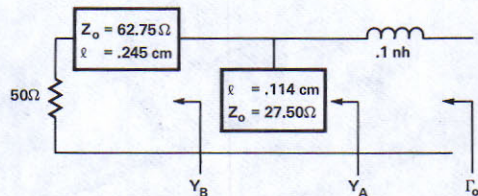


Figure 1. Input Matching on Smith Chart (Z/Y) and Resultant Input Circuit

$$Z_A = 8.76 - j\,17.22 - j\,7.5 = 8.76 - j\,24.72$$

$$Y_A = \frac{1}{Z_A} = 0.0127 + j\,0.0359$$

1. The first element, a quarter wave transformer, moves us out on the real axis to the conductance circle of Y_A. The characteristic impedance is:

$$Z_B = \sqrt{50 \times \frac{1}{(0.0127)}} = 62.75\ \Omega$$

A quarter wavelength on 25 mil alumina, (ϵ_r = 9.9) at 12 GHz for Z = 62.75 is:

$$\ell = \frac{C}{4f}\,V_r = \frac{3 \times 10^{10}}{4\,(12 \times 10^9)}\,(0.393) = 0.245\text{ cm}$$

2. The next element matches the reactive component. This is done with an open circuit stub. An open circuit

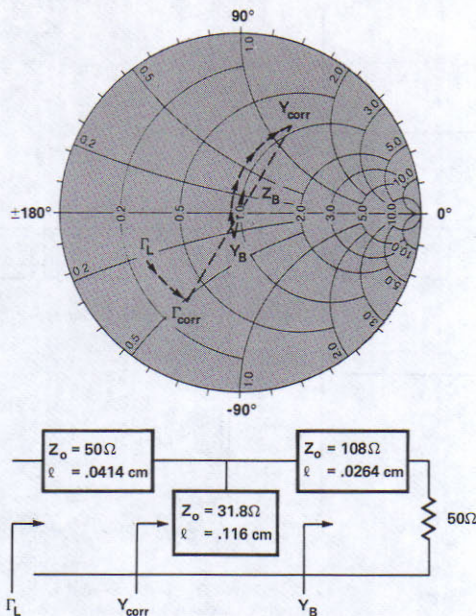


Figure 2. Output Matching on Smith Chart (Z/Y) and Resultant Output Circuit

stub λ/8 in length is capacitive with a susceptance equal to the characteristic admittance $Y_{oc} = Y_o = B$.

$$B = Y_o = (1.82)\ 20 \text{ mmhos} = 36.4 \text{ mmhos}$$

$$Z_o = \frac{1}{B} = 27.47\ \Omega$$

An eighth wavelength on alumina at 12 GHz for an impedance of 27.50Ω is:

$$\ell = \frac{C}{8f}\ V_r = \frac{3 \times 10^{10}}{8\ (12 \times 10^9)}\ (.365) = .114 \text{ cm}$$

This completes the input matching circuit.

Output Matching Circuit

To provide a bonding pad on the substrate, a rotation of 15.5° electrical length along the 50Ω line was included. The new impedance we want to design to is Z_{corr} (Figure 2).

$$\Gamma_L = .570 \angle -152^\circ$$

$$\Gamma_{corr} = .570 \angle -121^\circ \quad \text{Reflection coefficient angle rotation} = 2\beta\ell = 31^\circ$$

$$Z_{corr} = 17.65 - j\ 25.55$$

$$Y_{corr} = 18.3 + j\ 26.5 \text{ mmhos}$$

On alumina, the electrical length for a 15.5° rotation on a 50Ω line is:

$$\ell = \frac{15.5^\circ}{\beta}\ V_r = \frac{15.5^\circ}{144}\ (.385) = .0414 \text{ cm}$$

1. The first element, from the 50Ω load, is a series transformer which matches 50Ω to the constant conductance circle of Y_{corr}. To provide tuning flexibility, the length of the transformer will be varied. This is accomplished by a very narrow transmission line loop as shown in Figure 3. A practical line width of 0.635 mm (Z_o = 108Ω, V_r = .412, on alumina) was chosen for this purpose. The length of the transmission line can be determined by solving for the angle in the transmission line formula. The real part of the transmission line formula (admittance) is:

$$G = \frac{Y_o^2\ Y_L\ (1 + \tan^2\theta)}{Y_o^2 + Y_L^2 \tan^2\theta} = 18.3 \text{ mmhos}$$

Solving for θ yields

$$\tan^2\theta = \frac{Y_o^2\ (Y_L - G)}{Y_L\ (GY_L - Y_o^2)} = \frac{(9.3)^2\ (20 - 18.3)}{20\ [(18.3)\ (20) - (9.3)^2]}$$

$$\tan^2\theta = .0263$$

$$\theta = 9.2^\circ$$

This angle corresponds to an electrical length (for Z_o = 108, V_r = .412) on alumina of

$$\ell = \frac{\theta}{\beta}\ V_r = \frac{9.2^\circ}{144}\ (.412) = .0264 \text{ cm}$$

The transformed admittance is:

$$Y_B = \frac{Y_o\ (Y_L + j\ Y_o \tan\theta)}{(Y_o + j\ Y_L \tan\theta)} = \frac{(9.3)\ [20 + j\ (9.3) \tan(9.2)]}{[9.3 + j\ (20) \tan(9.2)]}$$

$$= 18.3 - j\ 4.9 \text{ mmhos}$$

2. The next element matches, B_T, the reactive component of Y_B to B_{corr}. This is accomplished by using an open circuit stub equal to λ/8 in length.

$$B_T = B_{corr} - B_B = 26.5 + 4.9 \text{ mmhos}$$

$$B_T = 31.4 \text{ mmhos}$$

$$Z_o = \frac{1}{B_T} = 31.8$$

A width of 0.136 cm corresponds to an impedance of 31.8Ω and phase velocity of .370 on alumina. An eighth wavelength on alumina, with Z_o = 31.8 at 12 GHz is:

$$\ell = \frac{\lambda}{8}\ V_r = \frac{2.5 \text{ cm}}{8}\ (.370) = .116 \text{ cm}$$

The completed 12 GHz amplifier circuit is shown in Figure 3.

Balanced stubs were used along the series transmission lines to minimize transition interactions.

Performance

The amplifier was constructed and measured for performance over the bandwidth described.

The noise figure is 3.1 dB at 12 GHz and less than 3.4 dB across the band (Figure 4). The associated gain is 7.5 dB at 12 GHz. Gain flatness is ±.25 dB.

P_{1dB} — Output power was measured with increasing input power. Power output for 1 dB gain compression is +12 dBm.

Third Order Intercept — Two fundamental signals, centered on each side of 11.950 GHz, are applied to the input of the amplifier. With a frequency separation of 20 MHz, third order distortion products are measured versus increasing fundamental input power. Lines were linearly extrapolated from the data and their intersection define the intercept point. The intercept point is +22 dBm.

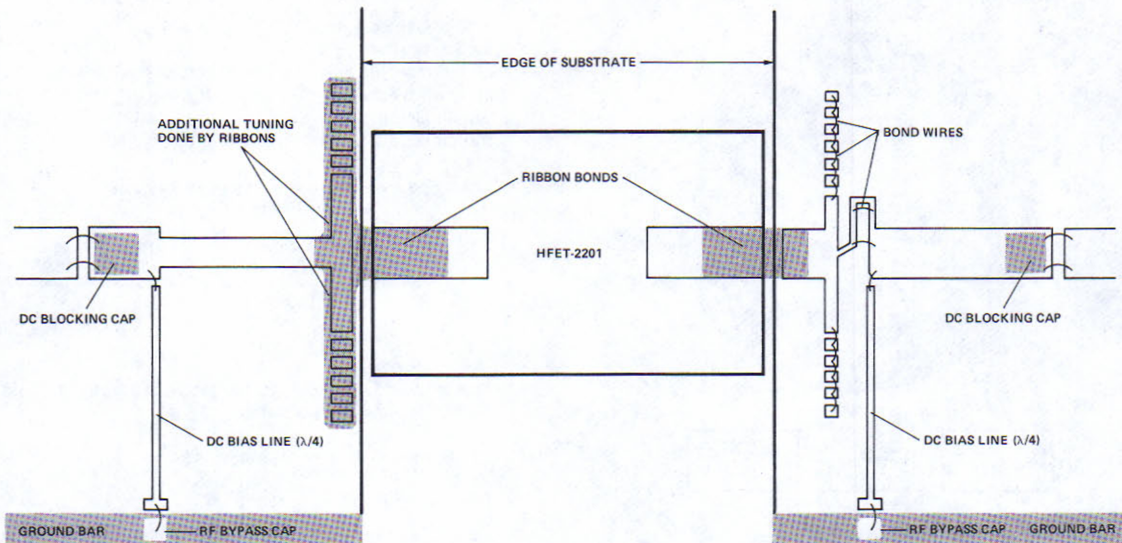


Figure 3. Completed 12 GHz Amplifier with DC Blocking and Bias

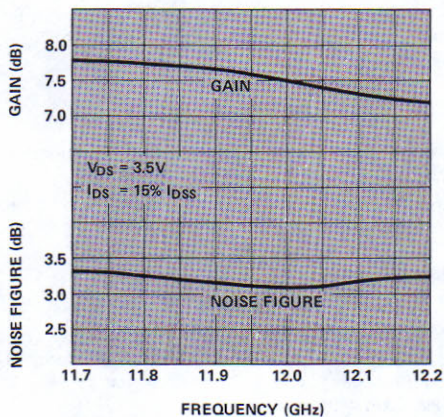


Figure 4. Associated Gain and Noise Figure vs. Frequency

Construction

The substrate material is Alumina. The relative dielectric constant (ϵ_r) is 9.9. Alumina was chosen because the high dielectric constant yields a smaller geometry.

DC bias was applied using high impedance quarter wavelength lines.

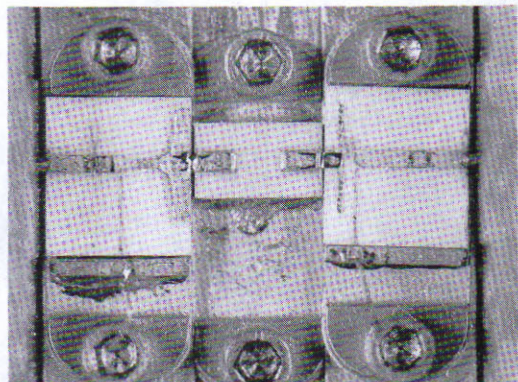


Figure 5. Close-up Photograph of the 12 GHz Low Noise Amplifier

REFERENCES

1. RT/Duroid manufactured by Rogers Corp., Chandler, Arizona.

The Design of GaAs FET Oscillators
(Portion of Application Note 978)

INTRODUCTION

The design technique for bipolar transistor oscillators proposed in Hewlett-Packard Application Note 975 is shown to be applicable to GaAs FET oscillators also. In order to compare GaAs FET and bipolar oscillators, 4.3 GHz oscillators using the HFET-1101 (1 micron gate length) and the HFET-2202 (0.5 micron gate length) were built with a topology similar to the bipolar HXTR-4101 oscillator described in AN 975. Phase noise is compared between different oscillators.

FET OSCILLATOR DESIGN

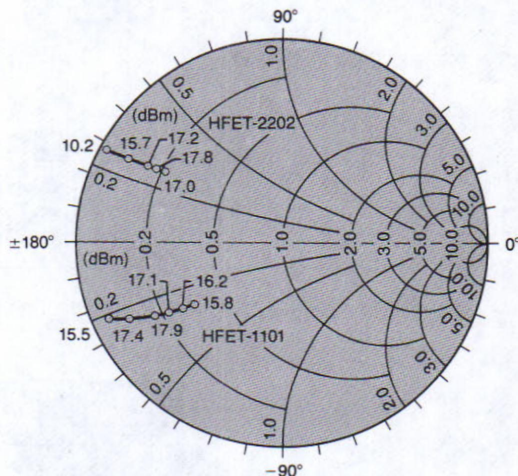
With the transistor represented by its measured S-parameters at 4.3 GHz, an initial topology using shorted 50Ω stubs in the source circuit and an open 50Ω stub attached to the gate was selected and computer optimized[1] in order to produce circuit dimensions that would provide an input impedance of −50Ω[2]. With this topology, however, there was no solution, so additional elements (open 50Ω shunt stubs) were utilized in the drain circuit. This topology provided solutions for both the HFET-2202 and HFET-1101.

These —50Ω microstrip networks were fabricated on RT/Duroid[3] 5880, FETs were installed and biased, and circuits were then analyzed on a Hewlett-Packard model 8410B network analyzer test system for optimum load impedance required to provide maximum oscillator power output at 4.3 GHz. To obtain this information the harmonic converter (8411A) was reversed so that the impedance observed on the polar display exhibited the impedance with its sign reversed. The incident and reflected powers were recorded as a function of incident power, and the impedance associated with each power level was noted. From this data the maximum added power (reflected-incident) and the related impedance were obtained. The power and impedance information are shown in Figure 1.

The displayed impedance at maximum added power is the optimum load impedance. The design was completed with the fabrication of matching networks involving two 50Ω open shunt stubs placed the required distance away from the reference plane of the impedance measurement.

OSCILLATOR PERFORMANCE

Circuits were then tested, and the HFET-1101 circuit oscillated without any tuning adjustment with an output power of 17.7 dBm. The HFET-2202 required slight adjustment of the gate and drain stubs after which it produced an output power of 17.6 dBm. The maximum added power for the −50Ω circuits were 17.9 and 17.8 dBm for the HFET-1101 and HFET-2202 respectively. This shows good agreement between measured and predicted power levels. A comparison of computed versus final circuit dimensions is shown in Figure 2.



FREQUENCY = 4.3 GHz		
	HFET-1101	HFET-2202
$V_{DS(V)}$	4.0	3.5
$I_{DS(mA)}$	45	84

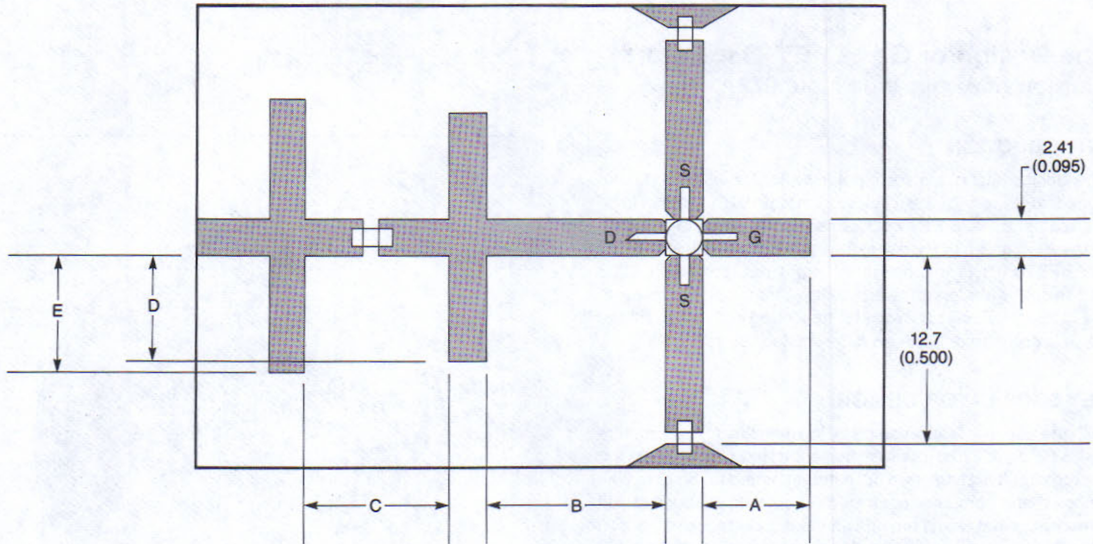
Figure 1. Load Impedance Versus Added Power for HFET-1101 and -2202 Non-Oscillating Circuits.

PHASE NOISE

Figure 3 compares the phase noise of these GaAs FET oscillators to that of a similarly designed HXTR-4101 oscillator (AN 975). The GaAs FET oscillators are about 16 dB noisier. This result is similar to that obtained for microstrip voltage controlled oscillators[4] at X-band.

CONCLUSIONS

The oscillator technique described in AN 975 for bipolar transistors is also applicable to GaAs FETs. FET oscillators do seem to have higher phase noise than bipolar oscillators; however, the FET oscillator noise appears to be more sensitive to the matching circuit. It was also observed that the 1 micron gate FET (HFET-1101) exhibited slightly lower phase noise than the half-micron device (HFET-2202).



	HFET-1101 LENGTH	HFET-2202 LENGTH	
	COMPUTED AND ACTUAL	COMPUTED	ACTUAL
A	8.03 (0.316)	7.62(0.300)	8.13(0.320)
B	14.0 (0.552)	14.0 (0.550)	14.0 (0.550)
C	8.18 (0.322)	14.0 (0.550)	14.0 (0.550)
D	6.63 (0.261)	7.65(0.301)	6.48(0.255)
E	5.44 (0.214)	6.50(0.256)	6.60(0.260)

DIMENSIONS IN MILLIMETERS (INCHES)
MATERIAL: RT/DUROID 5880
THICKNESS: 0.079(0.031)

Figure 2. Computed and Actual Dimensions for the HFET-1101 and -2202 Oscillators.

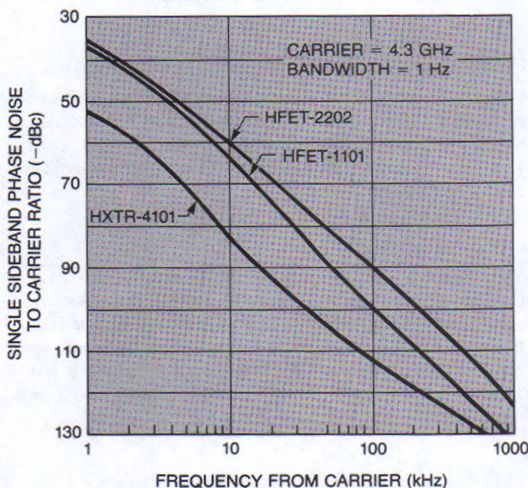


Figure 3. Phase Noise of HFET-1101, -2202 and HXTR-4101 Oscillators.

REFERENCES

1. Compact Engineering, Inc., a Division of CGIS, 1131 San Antonio Road, Palo Alto, CA 94303.
2. Hewlett-Packard Application Note 976, "A 4.3 GHz Oscillator Using The HXTR-4101 Bipolar Transistor."
3. Rogers Corporation, Chandler, Arizona.
4. Edward C. Niehenke and Ricky D. Hess, "A Microstrip Low-Noise X-Band Voltage Controlled Oscillator," IEEE Trans. MTT, Vol. MTT-27, No. 12, pp 1075-1079 (December 1979).
5. Dieter Scherer, "Learn About Low Noise Design," Microwaves, Vol. 18, No. 4, pp 120-122 (April 1979).

Bipolar Transistors

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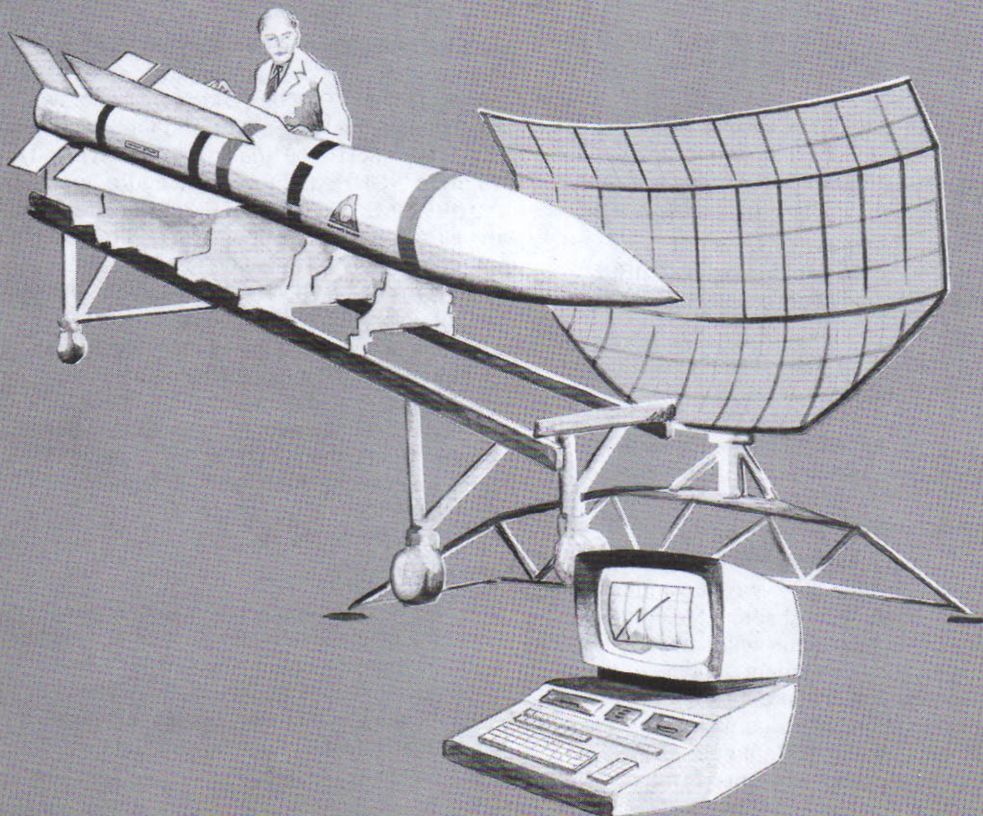


Silicon Bipolar Transistors

The Silicon Bipolar transistor is a semiconductor device, with amplification due to current gain. The advantages silicon bipolar transistors have over other transistor types are mature technology (both in the understanding of the device physics and the device design), low cost, and proven reliability. Therefore, silicon bipolar transistors offer designers a familiar, reliable, cost effective solution to many of their design needs.

The Hewlett-Packard silicon bipolar transistors are each characterized using standard D.C. and R.F. specifications. The typical D.C. specifications include pertinent junction parameters (such as junction breakdown voltages and leakage currents) and Beta (h_{FE}). The R.F. parameters include the following:

$G_{a(max)}$ (Maximum Available Gain) — When a device is unconditionally stable (i.e., no load with a positive real part will cause oscillations) and the input and output are simultaneously conjugately matched to 50Ω, the resultant gain is a maximum and is called $G_{a(max)}$.

F_{MIN} (Minimum Noise Figure) — The lowest possible noise figure of the transistor when properly biased and matched for low noise operation.

G_a (Associated Gain) — The resultant gain when properly biased and matched for low noise operation. This gain is less than $G_{a(max)}$.

P_{1dB} (Power Output at 1 dB Gain Compression) — When the input power increases until the small signal tuned gain compresses by 1 dB, the resultant output power is called P_{1dB}.

S-Parameters — S-parameters are four measurable normalized vector quantities that relate to reflection coefficients and gains. The four S-parameters are described as follows; S_{11}, the input reflection coefficient; S_{21}, the forward transmission coefficient (gain); S_{12}, the reverse transmission coefficient (isolation), S_{22}, the output reflection coefficient.

Included in the data sheets are two tables which distinguish between the different "Maximum Ratings" conditions. The "Absolute Maximum Ratings" are those conditions which, when exceeded, will cause permanent damage to the device. These are the standard maximum ratings used for derating purposes. The "Recommended Maximum Continuous Operating Conditions" are those conditions within which the stated reliability conditions are effective.

The Hewlett-Packard Silicon Bipolar product line has five basic transistor types; the HXTR-2000 series, the new HXTR-3000 series, the new HXTR-4101, the HXTR-5000 series, and the HXTR-6000 series.

The HXTR-2000 Series

The HXTR-2000 series is designed for general gain amplifier stage requirements. The HXTR-2000 series devices have 2μm emitter widths, and 450 mW of total device dissipation. These transistors have high maximum available gain (typically 17.5 dB at 2 GHz), high linear output power (P_{1dB} typically 20 dBm at 2 GHz) with a small degradation in noise figure (typically 2.2 dB at 2 GHz). The HXTR-2000 series is offered in two rugged hermetic packages, the HPAC-100 and the HPAC-70GT. The HXTR-2101 is packaged in the HPAC-100, and the HXTR-2102 is packaged in the HPAC-70GT. The HXTR-2001, the transistor chip, is also available for hybrid applications (see Hybrid Applications section). All of the HXTR-2000 series devices are characterized from 100 MHz to 6.5 GHz.

The HXTR-3000 Series

The HXTR-3000 series devices are designed for high volume, low cost applications in the UHF range. The HXTR-3000 series consists of two basic chips; the HXTR-3001 and the HXTR-3002. The HXTR-3001 has high gain (typically 16 dB at 2 GHz), and low noise figure (typically 2.2 dB at 2 GHz). The HXTR-3001 is offered in the HPAC-100X (a low cost, rugged metal/ceramic package) as the HXTR-3101 and the HXTR-3103. The HXTR-3002 has high linear output power (typically 21 dBm at 1000 MHz) and high associated 1 dB compressed gain (typically 11.5 dB at 1000 MHz). The HXTR-3002 is also offered in the HPAC-100X, as the HXTR-3102 and the HXTR-3104. Both chip products, the HXTR-3001 and the HXTR-3102 are available for hybrid applications. All of the HXTR-3000 series devices are characterized from 100 MHz to 6 GHz.

The HXTR-4101

The HXTR-4101 is designed and characterized for common-base oscillator transistor applications. The device uses the HXTR-2001 chip packaged in the HPAC-100. The HXTR-4101 has typical output power (oscillator power) of 20 dBm at 4.3 GHz. This device is characterized from 1 GHz to 12 GHz.

The HXTR-5000 Series

The HXTR-5000 series devices are designed for those applications where high linear output is required. The HXTR-5000 series consists of two basic transistor chips, the HXTR-5001 and the HXTR-5002. Both transistor chips have 2 μm emitter widths and Ta_2N ballast resistors. The HXTR-5001 has a total device dissipation of 700 mW, while the HXTR-5002 has a device dissipation of 2.7 W. The HXTR-5001 has higher linear output power than the HXTR-2000 series (P_{1dB} typically 23 dBm at 2 GHz), and high associated 1 dB compressed gain (typically 13.5 dB of 2 GHz). The HXTR-5001 is offered in the HPAC-100 and the HPAC-200. The HXTR-5101 is in the HPAC-100, and the HXTR-5103 is in the HPAC-200. The HXTR-5002 has the highest linear output power of the transistor product line (typically 29 dBm at 2 GHz) and high associated 1 dB compressed gain (typically 12.5 dB gain at 2 GHz). The HXTR-5002 devices are offered in the hermetic packages HPAC-200 GB/GT and the HPAC-200. The HXTR-5102 is packaged in the HPAC-200 GB/GT, and the HXTR-5104 is packaged in the HPAC-200. Both chip transistors, the HXTR-5001 and HXTR-5002, are available for hybrid applications. All the HXTR-5000 series devices are characterized from 100 MHz to 6 GHz.

The HXTR-6000 Series

The HXTR-6000 series devices are designed for those applications where low noise performance is a premium. These devices stem from two basic transistor chips, the HXTR-6001 and the HXTR-2001. The transistors using the HXTR-6001 have the lowest noise figure and the highest associated gain. The HXTR-6001 transistor has a 1 μm emitter width, a typical noise figure of 1.7 dB (at 2 GHz) with 13 dB of associated gain, and 150 mW of total device dissipation. The HXTR-6001 transistors are offered in the HPAC-70GT and the HPAC-100. The HXTR-6101 and the HXTR-6102 (low noise selection of the HXTR-6101) are offered in the HPAC-70GT. The HXTR-6103 and the HXTR-6104 (low noise selection of the HXTR-6103) are in the HPAC-100. The chip, the HXTR-6001, is available for hybrid applications (see Hybrid Applications Section). The HXTR-6105 and the HXTR-6106 use the HXTR-2001 chip. The HXTR-6105 is packaged in the HPAC-100, and the HXTR-6106 is packaged in the HPAC-70GT. The HXTR-6105 and the HXTR-6106 are low noise selections of the HXTR-2101 and the HXTR-2102 respectively. These devices are all characterized from 100 MHz to 6 GHz, or higher.

Silicon Bipolar Transistor Selection Guide

LOW NOISE TRANSISTORS (Guaranteed RF Performance)

Part Number HXTR-	Typical Noise Figure	Typical Associated Gain	Frequency	Package HPAC-	Chip* Equivalent HXTR-	Page Number
6101 (2N6617)	2.8 dB (3.0)	9.0 dB (8.0)	4 GHz	70 GT	6001	57
6102 (2N6742)	2.5 dB (2.7)	9.0 dB (8.0)	4 GHz	70 GT	6001	57
6103 (2N6618)	1.8 dB (2.2)	12.0 dB (11.0)	2 GHz	100	6001	60
6104 (2N6743)	1.4 dB (1.6)	14.0 dB (13.0)	1.5 GHz	100	6001	63
6105	3.8 dB (4.2)	9.0 dB (8.0)	4 GHz	100	2001	65
6106	2.5 dB (2.7)	11.5 dB (10.0)	2 GHz	70 GT	2001	68

OSCILLATOR TRANSISTOR

Part Number HXTR-	Minimum Power Output		Frequency	Package HPAC-	Chip* Equivalent HXTR-	Page Number
4101	19 dBm		4.3 GHz	100	2001	38

GENERAL PURPOSE TRANSISTORS (Guaranteed RF Performance)

Part Number HXTR-	Typical Gain	Typical P_{1dB}	Frequency	Package HPAC-	Chip* Equivalent HXTR-	Page Number
2101 (2N6679)	10.5 dB	18.5 dB	4 GHz	100	2001	25
2102	15.0 dB	20.0 dBm	2 GHz	70 GT	2001	27
3101	19.5 dB		1 GHz	100X	3001	29
3103 (2N6838)	15.0 dB (13.5)	16.0 dBm	1 GHz	100X	3001	33

LINEAR POWER TRANSISTORS (Guaranteed RF Performance)

Part Number HXTR-	Typical P_{1dB}	Typical G_{1dB}	Frequency	Package HPAC-	Chip* Equivalent HXTR-	Page Number
3102	21.0 dBm	11.5 dB	1 GHz	100X	3002	31
3104 (2N6839)	21.0 dBm (19.0)	16.0 dB (14.0)	1 GHz	100X	3002	36
5101 (2N6701)	22.0 dBm (21.0)	7.5 dB (6.5)	4 GHz	100	5001	41
5102	27.5 dBm (26.5)	7.0 dB (6.0)	4 GHz	200 GB/GT	5002	45
5103 (2N6741)	23.0 dBm (22.0)	11.0 dB (9.5)	2 GHz	200	5001	49
5104	29.0 dBm (28.0)	9.0 dB (8.0)	2 GHz	200	5002	53

Hewlett-Packard also supplies microwave bipolar transistors from the 35800 series for use in existing systems. Designers selecting transistors for use in new designs are encouraged to consider the superior performance of the HXTR series of devices available from Hewlett-Packard.

*For more detailed bipolar chip transistor information, see page 163 of "Devices for Hybrid Integrated Circuits" section.

HEWLETT PACKARD

GENERAL PURPOSE TRANSISTOR

2N6679 (HXTR-2101)

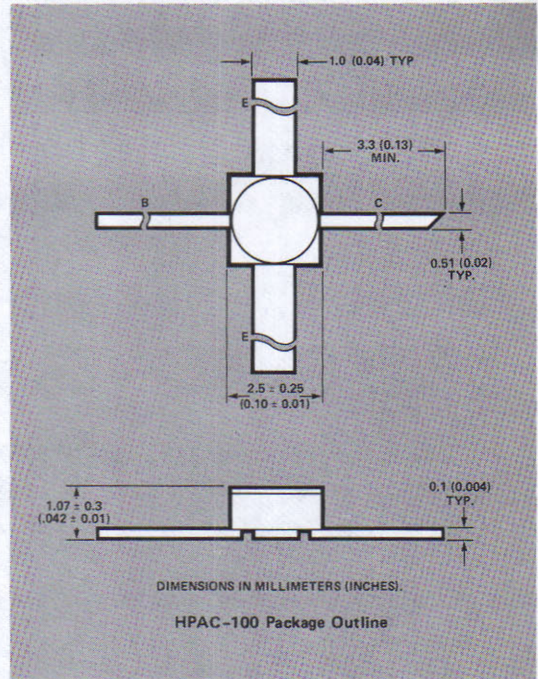
Bipolar Transistors

Features

HIGH GAIN
10.5 dB Typical at 4 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE



HPAC-100 Package Outline

Description

The 2N6679 (HXTR-2101) is an NPN bipolar transistor designed for high gain and output power at 4 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with a dielectric scratch protection over its active area.

The 2N6679 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE}=25°C

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage I_C=100μA	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at V_{CE}=15V	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at V_{CB}=15V	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio V_{CE}=15V, I_C=15mA	3076.1*	–	50	120	220
G_T	Tuned Gain		dB	9.0	10.5	
P_{1dB}	Power Output at 1 dB Compression Bias Conditions for Above: V_{CE}=15V, I_C=25mA, Frequency = 4 GHz		dBm		18.5	

*300 μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage [2]	25V
V_{CEO}	Collector to Emitter Voltage [2]	16V
V_{EBO}	Emitter to Base Voltage [2]	1.0V
I_C	DC Collector Current [2]	35mA
P_T	Total Device Dissipation [3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce device median time to failure (MTTF) of 3.5×10^6 hours at $T_J = 125°$ C (based on Activation Energy = 1.1 eV).
2. $T_{CASE} = 25°$ C.
3. Derate at 4.8 mW/° C, $T_C \geq 106°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

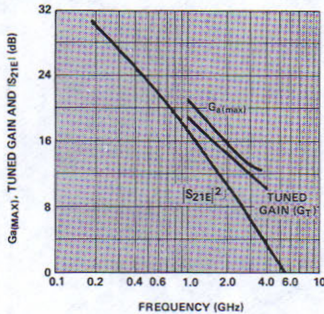


Figure 1. Typical $G_{a(MAX)}$ and Tuned Gain vs. Frequency at V_{CE}=15V, I_C=25 mA

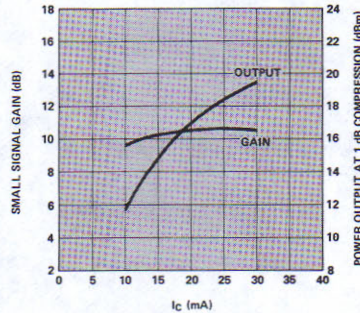


Figure 2. Typical Power Output at 1 dB Compression and Small Signal Gain vs. Collector Current at 4 GHz for V_{CE} = 15V.

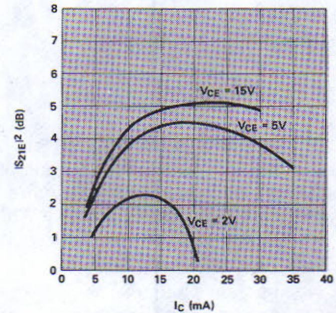


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 4 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 25mA

Freq. (MHz)	S11 Mag.	S11 Ang.	S21 (dB)	S21 Mag.	S21 Ang.	S12 (dB)	S12 Mag.	S12 Ang.	S22 Mag.	S22 Ang.
100	0.59	-66	30.8	34.6	146	-40.0	0.01	69	0.86	-18
500	0.58	-150	22.1	12.7	96	-33.2	0.02	44	0.51	-27
1000	0.59	-175	16.7	6.86	78	-30.5	0.03	51	0.44	-32
1500	0.59	173	13.3	4.61	64	-28.0	0.04	55	0.45	-39
2000	0.60	162	11.0	3.53	53	-25.7	0.05	55	0.44	-49
2500	0.61	156	8.9	2.79	43	-24.2	0.06	55	0.47	-60
3000	0.62	146	7.3	2.32	33	-22.6	0.07	56	0.48	-67
3500	0.63	139	5.9	1.96	22	-21.2	0.09	53	0.52	-79
4000	0.62	131	4.8	1.73	11	-19.7	0.10	50	0.55	-84
4500	0.61	123	3.5	1.50	1	-18.8	0.12	48	0.59	-93
5000	0.60	116	2.6	1.35	-9	-17.0	0.14	44	0.65	-102
5500	0.62	109	1.8	1.23	-19	-15.9	0.16	36	0.66	-113
6000	0.62	103	0.9	1.11	-28	-15.6	0.17	32	0.66	-123
6500	0.62	93	0.0	1.02	-37	-13.7	0.20	28	0.67	-131

HEWLETT PACKARD

GENERAL PURPOSE TRANSISTOR

HXTR-2102

Features

HIGH GAIN

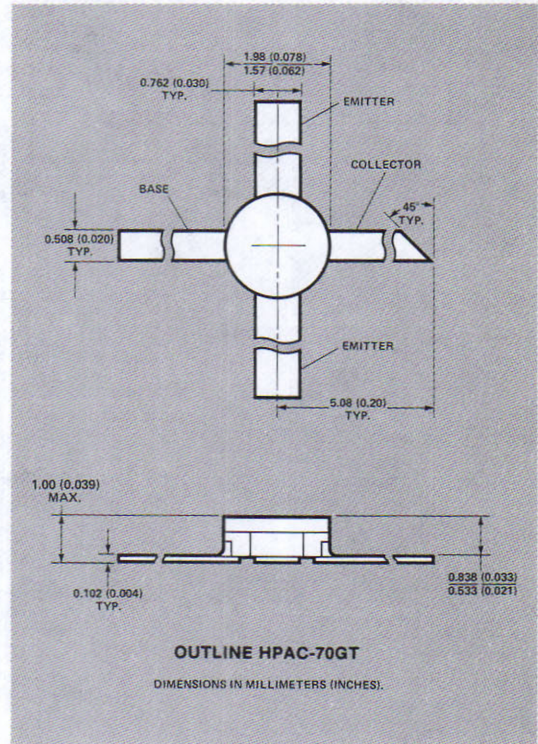
15 dB Typical at 2 GHz

11 dB Typical at 4 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE

Co-fired Metal/Ceramic Construction



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Description

The HXTR-2102 is an NPN bipolar transistor designed for high gain and wide dynamic range up to 6 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with a dielectric scratch protection over its active area.

The HXTR-2102 is supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$	3076.1*	—	50	120	220
G_T	Tuned Gain f=2 GHz 4 GHz		dB	13	15 11	
P_{1dB}	Power Output at 1 dB Compression f=2 GHz 4 GHz		dBm		20 18.5	
	Bias Conditions for Above: $V_{CE} = 15V$, $I_C = 25mA$					

*300μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65°C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce device median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 5.4 mW/° C, $T_C \geq$ 117° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

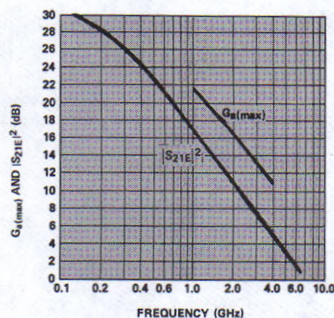


Figure 1. Typical $G_{a(max)}$ and $|S_{21E}|^2$ vs. Frequency at V_{CE}=15V, I_C=25 mA.

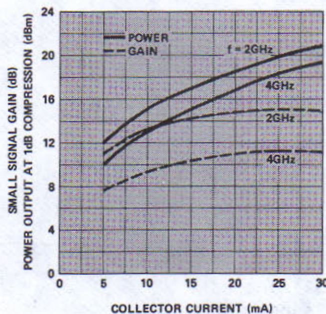


Figure 2. Typical Power Output at 1dB Compression and Small Signal Gain vs. Current for V_{CE}=15V

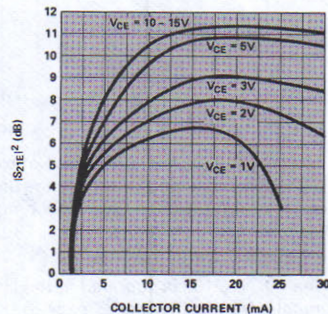


Figure 3. Typical $|S_{21E}|^2$ vs. Current at 2 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 25mA

Freq. (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} (dB)	S_{21} Mag.	S_{21} Ang.	S_{12} (dB)	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.63	-58	30.5	33.4	149	-39.2	0.011	62	0.88	-16
200	0.63	-99	28.4	26.2	128	-35.9	0.016	49	0.72	-25
300	0.64	-122	26.1	20.3	115	-34.9	0.018	45	0.61	-28
400	0.64	-136	24.2	16.2	107	-33.6	0.021	42	0.54	-29
500	0.64	-146	22.6	13.4	101	-32.8	0.023	42	0.50	-31
600	0.64	-153	21.2	11.5	96	-32.4	0.024	43	0.48	-32
700	0.64	-158	19.9	9.9	92	-32.0	0.025	43	0.47	-33
800	0.64	-162	18.8	8.8	88	-31.7	0.026	45	0.47	-34
900	0.64	-166	17.8	7.8	85	-31.4	0.027	44	0.48	-34
1000	0.64	-170	16.9	7.0	83	-30.8	0.029	46	0.47	-35
1500	0.66	179	13.5	4.7	70	-29.1	0.035	49	0.44	-40
2000	0.65	172	11.1	3.6	60	-27.1	0.044	53	0.46	-50
2500	0.67	165	9.1	2.9	50	-25.7	0.052	55	0.47	-59
3000	0.64	161	7.6	2.4	40	-24.3	0.061	57	0.52	-66
3500	0.72	156	6.4	2.1	32	-23.3	0.068	53	0.51	-79
4000	0.69	149	5.3	1.8	22	-22.6	0.074	48	0.56	-85
4500	0.70	141	4.4	1.7	14	-21.8	0.081	44	0.55	-92
5000	0.72	136	3.3	1.5	6	-21.3	0.086	39	0.58	-101
5500	0.70	128	2.5	1.3	-3	-20.7	0.092	34	0.62	-109
6000	0.75	122	1.7	1.2	-11	-20.1	0.098	30	0.63	-118
6500	0.70	119	0.8	1.1	-20	-19.6	0.105	26	0.70	-127

HEWLETT PACKARD

LOW COST GENERAL PURPOSE TRANSISTOR

HXTR-3101

Bipolar Transistors

Features

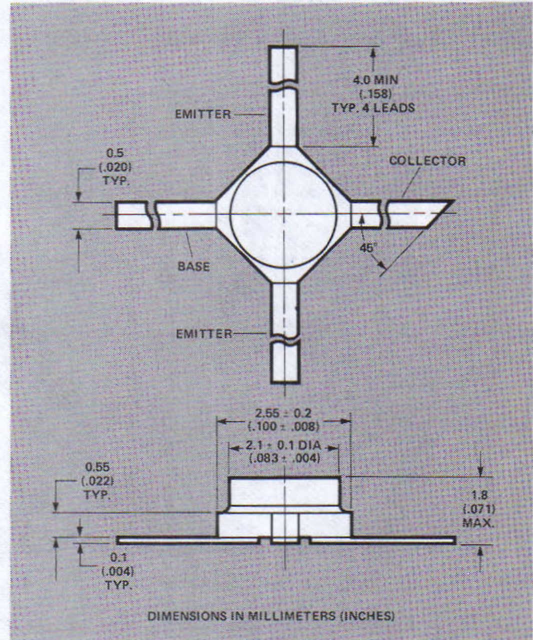
HIGH GAIN
19.5 dB Typical at 1 GHz

LOW NOISE FIGURE
1.8 dB Typical at 1 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE

LOW COST



OUTLINE HPAC-100X
Product Identification = U

Description

The HXTR-3101 is a low cost NPN bipolar transistor designed for high gain and wide dynamic range up to 4000 MHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes self-alignment, ion implantation techniques, and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area.

The HXTR-3101 is supplied in the HPAC-100X, a rugged metal/ceramic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the electrical test conditions of MIL-STD-750.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C = 100\ \mu A$	3001.1*	V	30		
I_{CBO}	Collector-Base Cuttoff Current at $V_{CE} = 15$ V	3036.1**	nA			500
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 10$ V, $I_C = 10$ mA	3076.1*		50		180
f_T	Gain Bandwidth Product at $V_{CE} = 10$ V, $I_C = 15$ mA		GHz		6	
$\|S_{21E}\|^2$	Transducer Gain at 1000 MHz at $V_{CE} = 10$ V, $I_C = 15$ mA		dB		15	
F_{MIN}	Minimum Noise Figure at 1000 MHz at $V_{CE} = 10$ V, $I_C = 10$ mA		dB		1.8	
MAG	Maximum Available Gain at 1000 MHz at $V_{CE} = 10$ V, $I_C = 15$ mA		dB		19.5	

*300 μs wide pulse measurement ≤ 2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions (1)

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	30mA
P_T	Total Device Dissipation	300mW
T_J	Junction Temperature (2)	200°C
T_{STG}	Storage Temperature	-65°C to +150°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (based on Activation Energy = 1.5 eV).
2. Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	18V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	50mA
P_T	Total Device Dissipation	600mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	200°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

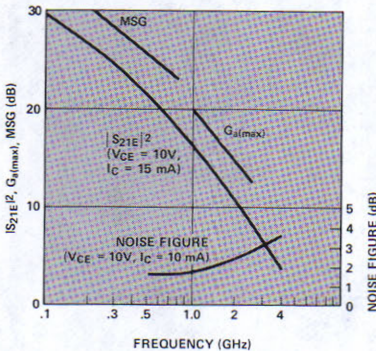


Figure 1. Typical $|S_{21E}|^2$, $G_{a(max)}$, Maximum Stable Gain (MSG), and Noise Figure vs. Frequency

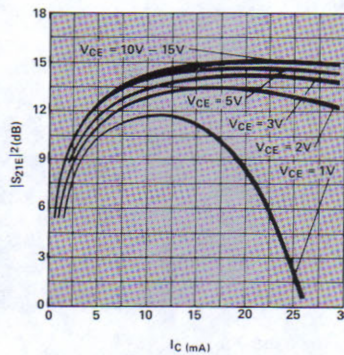


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1000 MHz

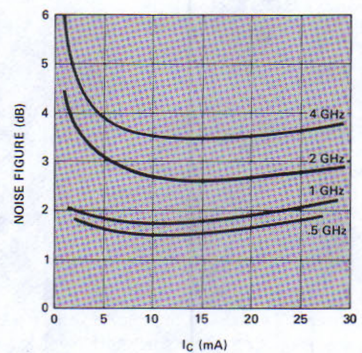


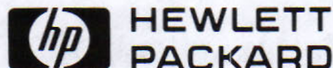
Figure 3. Typical Noise Figure vs. Collector Current (V_{CE} = 10V)

Typical S-Parameters (V_{CE} = 10 V, I_C = 10 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.705	-50	27.7	24.266	149	-36.7	0.015	60	0.903	-20
300	0.606	-110	23.5	14.962	116	-30.4	0.030	43	0.624	-36
500	0.565	-139	20.1	10.116	101	-28.9	0.036	41	0.499	-40
800	0.559	-162	16.5	6.683	89	-27.4	0.043	43	0.430	-41
1000	0.571	-169	14.5	5.330	78	-25.7	0.052	44	0.408	-43
1500	0.574	174	11.2	3.627	63	-23.6	0.066	48	0.394	-48
2000	0.591	161	8.9	2.774	49	-21.9	0.080	48	0.392	-57
3000	0.619	143	5.7	1.936	25	-18.8	0.115	45	0.427	-81
4000	0.639	125	3.4	1.488	1	-16.2	0.155	39	0.470	-107

(V_{CE} = 10 V, I_C = 15 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.641	-60	29.5	29.854	144	-37.6	0.013	57	0.863	-23
300	0.565	-122	24.5	16.788	112	-31.8	0.026	44	0.556	-38
500	0.551	-149	20.7	10.839	98	-30.1	0.031	44	0.444	-40
800	0.553	-168	17.1	7.161	87	-28.1	0.039	50	0.387	-41
1000	0.560	-175	15.1	5.709	77	-26.4	0.048	49	0.363	-42
1500	0.564	171	11.8	3.869	62	-23.6	0.066	54	0.356	-47
2000	0.583	159	9.4	2.955	49	-21.6	0.083	52	0.354	-56
3000	0.611	142	6.3	2.058	26	-18.4	0.120	47	0.389	-81
4000	0.633	124	4.0	1.587	2	-15.9	0.160	39	0.431	-106



LOW COST GENERAL PURPOSE LINEAR POWER TRANSISTOR

HXTR-3102

Bipolar Transistors

Features

HIGH P_{1dB} LINEAR POWER
21 dBm Typical at 1 GHz

HIGH G_{1dB} GAIN
11.5 dB Typical at 1 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE

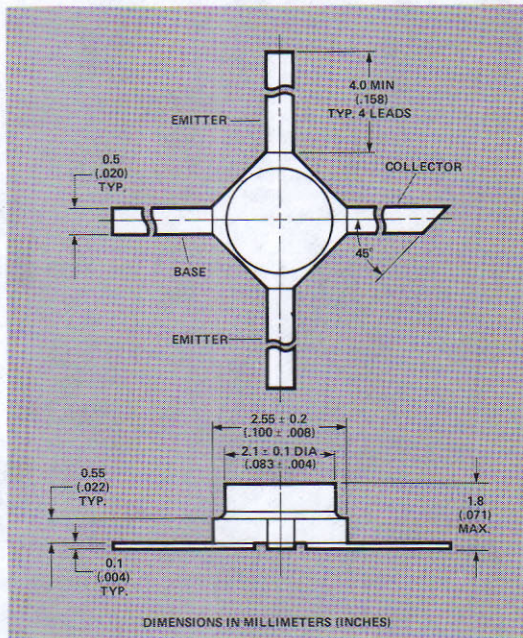
EMITTER BALLAST RESISTORS

LOW COST

Description

The HXTR-3102 is a low cost NPN bipolar transistor designed for high linear output power and high gain up to 4000 MHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes self-alignment, ion implantation techniques, and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N emitter ballast resistors.

The HXTR-3102 is supplied in the HPAC-100X, a rugged metal/ceramic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the electrical test conditions of MIL-STD-750.



OUTLINE HPAC-100X
Product Identification = B

Electrical Specifications at T_{CASE} = 25°C

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C = 100 μA	3001.1*	V	35		
I_{CBO}	Collector-Base Cutoff Current at V_{CE} = 20 V	3036.1**	nA			200
h_{FE}	Forward Current Transfer Ratio at V_{CE} = 15 V, I_C = 30 mA	3076.1*		15		75
f_T	Gain Bandwidth Product at V_{CE} = 15 V, I_C = 30 mA		GHz		6	
$\|S_{21E}\|^2$	Transducer Gain at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dB		12.5	
P_{1dB}	Power Output at 1 dB Compression at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dBm		21	
G_{1dB}	Associated at 1 dB Compression Gain at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dB		11.5	

*300 μs wide pulse measurement ≤ 2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions(1)

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.0V
I_C	DC Collector Current	50 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature[2]	200° C
T_{STG}	Storage Temperature	-65° C to +150° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (based on Activation Energy = 1.5 eV).
2. Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	25V
V_{EBO}	Emitter to Base Voltage	3.5V
I_C	DC Collector Current	100mA
P_T	Total Device Dissipation	700mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	200° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

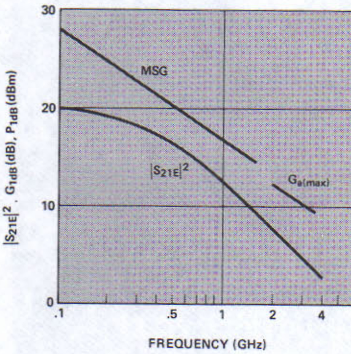


Figure 1. Typical $|S_{21E}|^2$, $G_{a(max)}$, and Maximum Stable Gain (MSG) vs. Frequency (V_{CE} = 15 V, I_C = 30 mA)

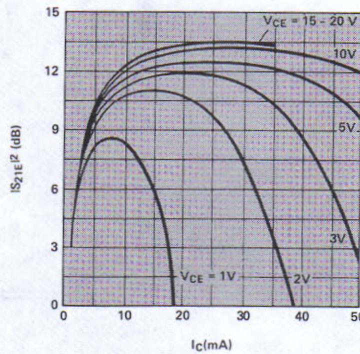


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1000 MHz

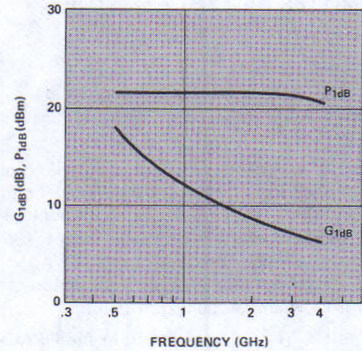


Figure 3. Typical Power Output at 1 dB Gain Compression vs. Frequency V_{CE} = 15 V, I_C = 30 mA

Typical S-Parameters (V_{CE} = 15 V, I_C = 20 mA)

	S11		S21			S12			S22	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.767	-19	18.9	8.810	165	-36.0	0.016	72	0.985	-10
300	0.699	-52	17.7	7.674	143	-27.0	0.045	60	0.892	-25
500	0.620	-79	16.1	6.383	126	-24.0	0.063	50	0.783	-35
800	0.556	-110	13.8	4.898	109	-22.2	0.078	41	0.654	-40
1000	0.548	-126	12.7	4.317	95	-21.0	0.089	34	0.598	-45
1500	0.523	-155	9.9	3.143	74	-20.2	0.098	30	0.525	-55
2000	0.513	-177	7.9	2.475	57	-19.7	0.103	29	0.489	-63
3000	0.534	156	5.1	1.792	30	-17.8	0.129	31	0.495	-85
4000	0.546	132	3.0	1.412	4	-15.6	0.166	29	0.522	-109

(V_{CE} = 15 V, I_C = 30 mA)

	S11		S21			S12			S22	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.777	-21	19.7	9.661	164	-35.9	0.016	71	0.985	-10
300	0.694	-57	18.3	8.222	139	-27.1	0.044	58	0.874	-27
500	0.606	-85	16.4	6.607	122	-24.4	0.060	48	0.757	-36
800	0.538	-116	13.9	4.955	105	-22.7	0.073	40	0.630	-40
1000	0.535	-131	12.7	4.296	92	-21.4	0.085	34	0.580	-44
1500	0.513	-159	9.8	3.086	72	-20.4	0.095	32	0.518	-53
2000	0.508	-180	7.7	2.415	55	-19.8	0.102	31	0.488	-62
3000	0.532	153	4.8	1.740	28	-17.8	0.129	33	0.500	-84
4000	0.546	130	2.7	1.362	3	-15.5	0.167	29	0.527	-108

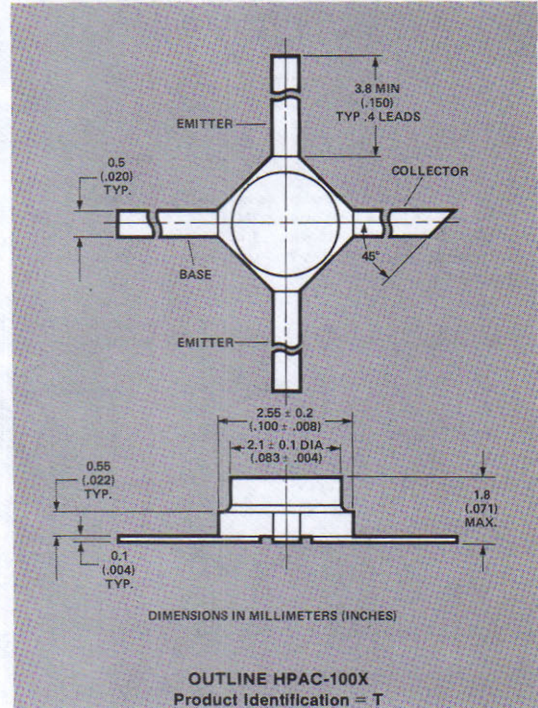
HEWLETT PACKARD

GENERAL PURPOSE TRANSISTOR

2N6838 (HXTR-3103)

Features

- **GUARANTEED TUNED NOISE FIGURE**
  2.3 dB Maximum at 1 GHz
- **HIGH GAIN**
  13.5 dB Minimum $|S_{21E}|^2$ at 1 GHz
- **HIGH GAIN BANDWIDTH PRODUCT**
  5.0 GHz Minimum f_T
- **WIDE DYNAMIC RANGE**
- **RUGGED HERMETIC PACKAGE**



OUTLINE HPAC-100X
Product Identification = T

Description

The HXTR-3103 is an NPN bipolar transistor designed for high gain and wide dynamic range up to 5 GHz. The device utilizes ion implantation, self alignment techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with a dielectric scratch protection over its active area.

The HXTR-3103 is supplied in the HPAC-100X, a rugged metal/ceramic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C = 100\ \mu A$	3001.1*	V	30		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C = 10$ mA	3011.1*	V	16		
I_{CBO}	Collector-Base Cutoff Current at $V_{CE} = 15V$	3036.1**	nA			50
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$	3041.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 10$ V, $I_C = 10$ mA	3076.1*		50		180
f_T	Gain Bandwidth Product at $V_{CE} = 10$ V, $I_C = 15$ mA		GHz	5.0	7.0	
$\|S_{21E}\|^2$	Transducer Gain at 1000 MHz at $V_{CE} = 10$ V, $I_C = 15$ mA		dB	13.5	15	
F_{MIN}	Minimum Noise Figure at 1000 MHz at $V_{CE} = 10$ V, $I_C = 10$ mA		dB		1.7	2.3
$F_{(50\Omega)}$	Noise Figure with 50 ohm Source at $V_{CE} = 10$ V, $I_C = 10$ mA, F = 1000 MHz		dB		2.1	
	500 MHz		dB		1.7	
P_{1dB}	Power Output at 1 dB Compression at $V_{CE} = 10$ V, $I_C = 15$ mA, 1000 MHz		dBm		16.0	
G_{1dB}	1 dB Gain Compression at $V_{CE} = 10$ V, $I_C = 15$ mA, 1000 MHz		dB		16.0	
C_{12E}	Reverse Transfer Capacitance $I_C = 0$ mA; $V_{CE} = 10$ V; f = 1 MHz		pF		0.33	

*300µs wide pulse measurement ≤ 2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions(1)

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	30 mA
P_T	Total Device Dissipation	400 mW
T_J	Junction Temperature[2]	200°C
T_{CASE}	Case Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +150°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125°C (based on Activation Energy = 1.1 eV).
2. A typical Θ_{JC} = 145°C/W (180°C/W Max) should be used for derating calculations.

Absolute Maximum Ratings*

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	18V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	50mA
P_T	Total Device Dissipation	600 mW
T_J	Junction Temperature	300°C
T_{CASE}	Case Temperature	200°C
T_{STG}	Storage Temperature	200°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

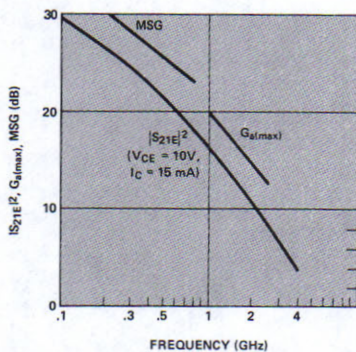


Figure 1. Typical $|S_{21E}|^2$, $G_{a\,(max)}$, Maximum Stable Gain (MSG).

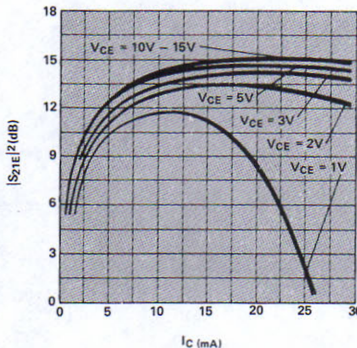


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1000 MHz.

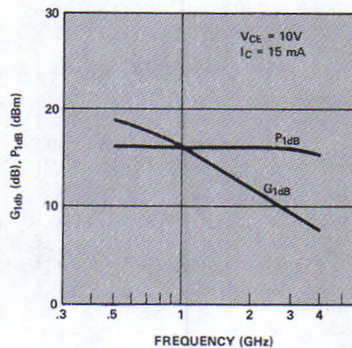


Figure 3. Typical Power Output at 1 dB Gain Compression vs. Frequency.

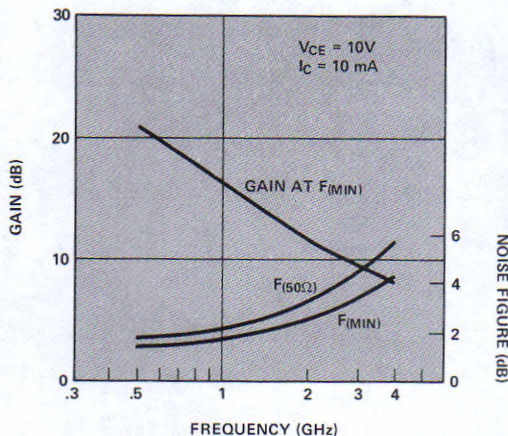


Figure 4. Typical Noise Figure vs. Frequency.

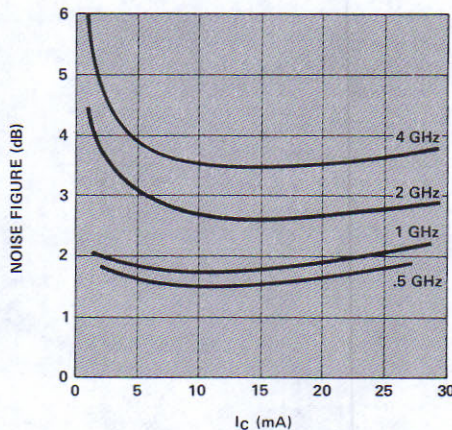


Figure 5. Typical Noise Figure vs. Collector Current.

Typical Noise Parameters

Freq. (GHz)	F_{MIN} (dB)	Γ_o Mag.	Γ_o Ang.	R_n (ohms)
.5	1.4	.121	96°	114.4
1.0	1.7	.301	121	15.2
2.0	2.5	.461	173	5.2
3.0	3.3	.553	-157	8.4
4.0	4.2	.648	-139	13.4

Table 1. Typical Noise Parameters at V_{CE} = 10 V, I_C = 10 mA.

Typical S-Parameters (V_{CE} = 10 V, I_C = 10 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.705	-50	27.7	24.266	149	-36.7	.015	60	.903	-20
200	.642	-86	25.6	19.055	129	-32.2	.025	49	.742	-31
300	.606	-110	23.5	14.962	116	-30.4	.030	43	.624	-37
400	.579	-127	21.6	12.023	108	-29.6	.033	41	.548	-38
500	.565	-139	20.1	10.116	102	-28.9	.036	41	.499	-40
600	.552	-149	18.7	8.610	97	-28.5	.038	42	.467	-40
700	.562	-157	17.5	7.499	93	-27.9	.040	43	.441	-42
800	.559	-162	16.5	6.683	89	-27.4	.043	44	.430	-42
900	.558	-168	15.5	5.957	85	-26.9	.045	46	.412	-43
1000	.571	-169	14.5	5.330	78	-25.7	.052	42	.408	-40
1500	.574	174	11.2	3.627	63	-23.6	.066	48	.394	-48
2000	.591	162	8.9	2.774	49	-21.9	.080	48	.392	-57
2500	.619	153	7.2	2.281	37	-20.4	.096	48	.390	-71
3000	.619	143	5.7	1.936	25	-18.8	.115	45	.427	-81
3500	.653	134	4.5	1.673	13	-17.5	.134	43	.424	-94
4000	.639	125	3.5	1.488	1	-16.2	.155	39	.470	-107

Typical S-Parameters (V_{CE} =V 10 V, I_C = 15 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.641	-60	29.5	29.854	144	-37.6	.013	57	.863	-24
200	.588	-98	26.9	22.131	124	-33.4	.021	47	.674	-34
300	.565	-122	24.5	16.788	112	-31.8	.026	44	.556	-38
400	.547	-138	22.4	13.183	104	-30.9	.029	43	.487	-39
500	.541	-149	20.7	10.839	98	-30.1	.031	44	.444	-40
600	.533	-157	19.3	9.226	94	-29.5	.033	47	.417	-40
700	.545	-164	18.1	8.035	90	-28.7	.037	49	.395	-41
800	.543	-168	17.1	7.161	87	-28.1	.039	50	.387	-41
900	.544	-173	16.1	6.383	84	-27.4	.043	52	.371	-42
1000	.560	-175	15.1	5.709	77	-26.4	.048	49	.363	-39
1500	.564	171	11.8	3.869	62	-23.6	.066	54	.356	-47
2000	.583	159	9.4	2.955	49	-21.6	.083	52	.354	-56
2500	.612	151	7.7	2.423	38	-20.0	.100	51	.353	-70
3000	.611	142	6.3	2.058	26	-18.4	.120	47	.389	-81
3500	.647	133	5.0	1.782	14	-17.1	.139	44	.385	-94
4000	.633	124	4.0	1.587	2	-15.9	.160	39	.431	-106

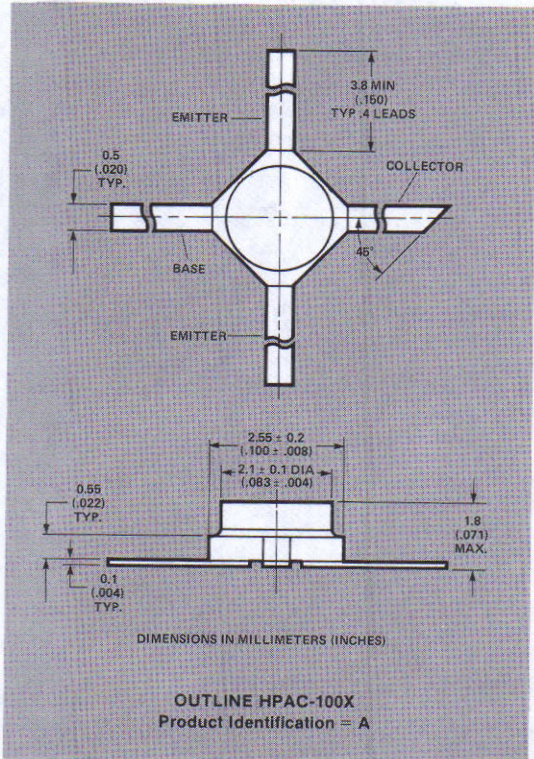
HEWLETT PACKARD

LINEAR POWER TRANSISTOR

2N6839 (HXTR-3104)

Features

- **GUARANTEED MINIMUM POWER OUTPUT AT 1 dB GAIN COMPRESSION**
  19.0 dBm Minimum at 1 GHz
- **GUARANTEED ASSOCIATED 1 dB COMPRESSED GAIN**
  14.0 dB Minimum at 1 GHz
- **HIGH GAIN BANDWIDTH PRODUCT**
  4.0 GHz Minimum f_T
- **WIDE DYNAMIC RANGE**
- **RUGGED HERMETIC PACKAGE**



OUTLINE HPAC-100X
Product Identification = A

Description

The HXTR-3104 is an NPN bipolar transistor designed for high output power and gain up to 4 GHz. Ion implantation, self-alignment techniques and Ti/Pt/Au metallization are used in its manufacture to produce excellent uniformity and reliability. The chip has a dielectric scratch protection over its active area and a Ta_2N ballast resistor for ruggedness.

The HXTR-3104 is supplied in the HPAC-100X, a rugged metal/ceramic package, and is capable of meeting the environmental requirements of MIL-S-19500 and test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE} = 25°C

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C = 100 μA	3001.1*	V	35		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C = 15 mA	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B = 30 μA	3026.1*	V	3.3		
I_{CBO}	Collector-Base Cutoff Current at V_{CE} = 20 V	3036.1**	nA			50
I_{CEO}	Collector-Emitter Leakage Current at V_{CE} = 15 V	3041.1	nA			75
h_{FE}	Forward Current Transfer Ratio at V_{CE} = 15 V, I_C = 30 mA	3076.1*		15		75
f_T	Gain Bandwidth Product at V_{CE} = 15 V, I_C = 30 mA		GHz	4.0	5.5	
$\|S_{21E}\|^2$	Transducer Gain at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dB	10.5	12.5	
P_{1dB}	Power Output at 1 dB Compression at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dBm	19.0	21	
G_{1dB}	Associated at 1 dB Compression Gain at 1000 MHz at V_{CE} = 15 V, I_C = 30 mA		dB	14.0	16.0	
C_{12E}	Reverse Transfer Capacitance I_C = 0 mA; V_{CE} = 10V; f = 1 MHz		pF		0.36	

*300μs wide pulse measurement ≤ 2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions(1)

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.0V
I_C	DC Collector Current	50mA
P_T	Total Device Dissipation	500 mW
T_J	Junction Temperature(2)	200° C
T_{CASE}	Case Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +150° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. A typical θ_{JC} = 130° C/W (165° C/W Max) should be used for derating calculations.

Absolute Maximum Ratings*

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	25V
V_{EBO}	Emitter to Base Voltage	3.5V
I_C	DC Collector Current	100mA
P_T	Total Device Dissipation	700mW
T_J	Junction Temperature	300° C
T_{CASE}	Case Temperature	200° C
T_{STG}	Storage Temperature	200° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

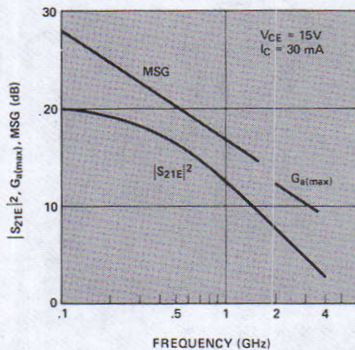


Figure 1. Typical $|S_{21E}|^2$, $G_{a\,(max)}$, and Maximum Stable Gain (MSG) vs. Frequency.

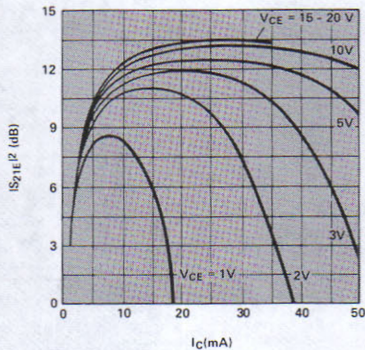


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1000 MHz.

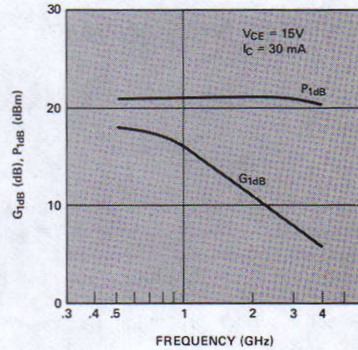


Figure 3. Typical Power Output at 1 dB Gain Compression vs. Frequency.

Typical S-Parameters (V_{CE} = 15 V, I_C = 20 mA)

Freq. (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} (dB)	S_{21} Mag.	S_{21} Ang.	S_{12} (dB)	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.767	-19	18.9	8.810	165	-36.0	0.016	72	0.985	-10
300	0.699	-52	17.7	7.674	143	-27.0	0.045	60	0.892	-25
500	0.620	-79	16.1	6.383	126	-24.0	0.063	50	0.783	-35
800	0.556	-110	13.8	4.898	109	-22.2	0.078	41	0.654	-40
1000	0.548	-126	12.7	4.317	95	-21.0	0.089	34	0.598	-45
1500	0.523	-155	9.9	3.143	74	-20.2	0.098	30	0.525	-55
2000	0.513	-177	7.9	2.475	57	-19.7	0.103	29	0.489	-63
3000	0.534	156	5.1	1.792	30	-17.8	0.129	31	0.495	-85
4000	0.546	132	3.0	1.412	4	-15.6	0.166	29	0.522	-109

Typical S-Parameters (V_{CE} = 15 V, I_C = 30 mA)

Freq. (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} (dB)	S_{21} Mag.	S_{21} Ang.	S_{12} (dB)	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.777	-21	19.7	9.661	164	-35.9	0.016	71	0.985	-10
300	0.694	-57	18.3	8.222	139	-27.1	0.044	58	0.874	-27
500	0.606	-85	16.4	6.607	122	-24.4	0.060	48	0.757	-36
800	0.538	-116	13.9	4.955	105	-22.7	0.073	40	0.630	-40
1000	0.535	-131	12.7	4.296	92	-21.4	0.085	34	0.580	-44
1500	0.513	-159	9.8	3.086	72	-20.4	0.095	32	0.518	-53
2000	0.508	-180	7.7	2.415	55	-19.8	0.102	31	0.488	-62
3000	0.532	153	4.8	1.740	28	-17.8	0.129	33	0.500	-84
4000	0.546	130	2.7	1.362	3	-15.5	0.167	29	0.527	-108

HEWLETT PACKARD

GENERAL PURPOSE OSCILLATOR TRANSISTOR

HXTR-4101

Features

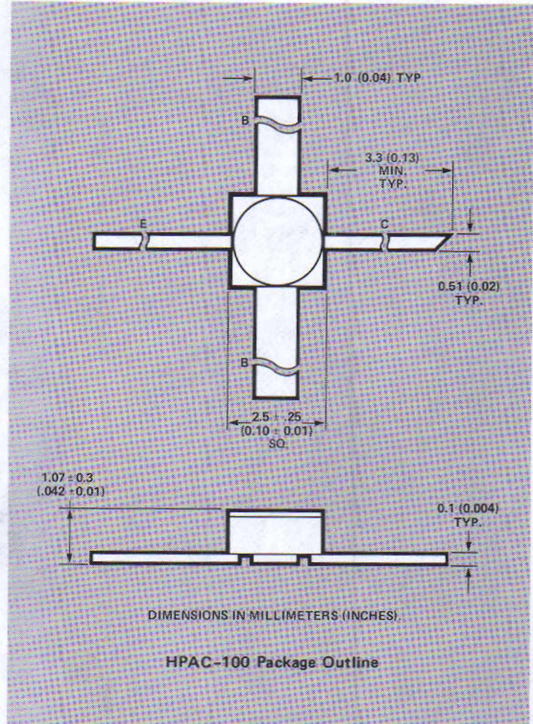
GUARANTEED OUTPUT POWER
19.0 dBm Minimum at 4.3 GHz

HIGH FREQUENCY PERFORMANCE
12 dBm Typical at 8 GHz

USABLE TO 10 GHz

CHARACTERIZED FOR OSCILLATOR APPLICATIONS

RUGGED HERMETIC PACKAGE



HPAC-100 Package Outline

Description

The HXTR-4101 is an NPN bipolar transistor designed for consistent high oscillator output. Each device is tested for specified oscillator performance at 4.3 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with dielectric scratch protection over its active area.

The HXTR-4101 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio $V_{CE} = 15V$, $I_C = 15mA$	3076.1*	—	50	120	220
P_{OSC}	Oscillator Output Power $V_{CB} = 15V$, $I_C = 30mA$ f = 3 GHz 4.3 GHz 6 GHz 8 GHz		dBm	19.0	21.5 20.5 17.0 12.0	
N/C	Phase Noise to Carrier Ratio at 1 KHz from the Carrier (SSB), f = 4.3 GHz		dBc/Hz		-50	

*300 μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (based on Activation Energy = 1.5 eV).
2. T_{CASE} = 25° C.
3. Derate at 4.8 mW/° C, $T_C \geq$ 106° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

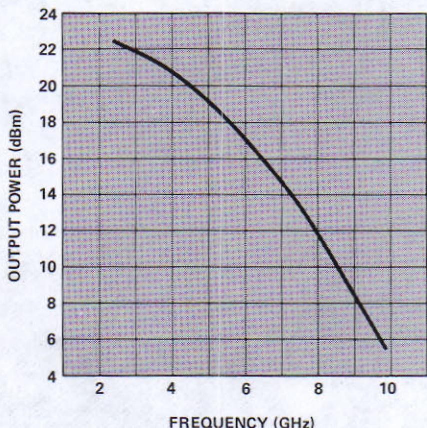


Figure 1. Typical Tuned Power Output vs. Frequency at V_{CB} = 15 V, I_C = 30 mA.

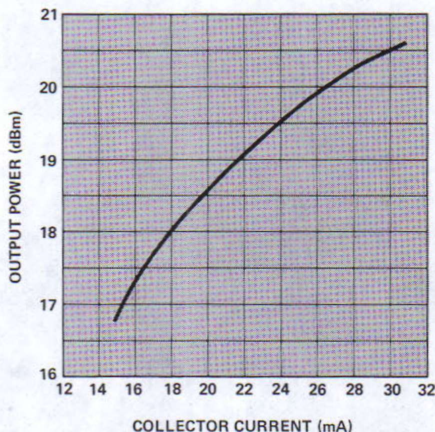


Figure 2. Typical Oscillator Power vs. Current for V_{CB} = 15 V at 4.3 GHz.

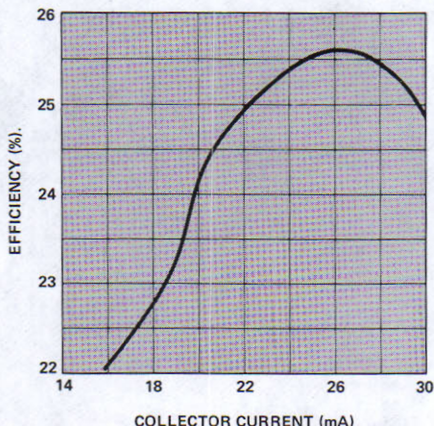


Figure 3. Typical Conversion Efficiency vs. Current for V_{CB} = 15 V at 4.3 GHz.

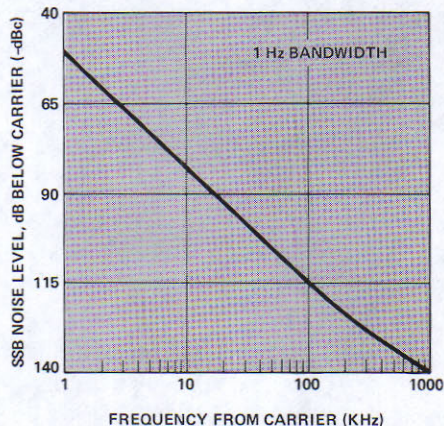


Figure 4. Typical Phase Noise to Carrier Ratio (N/C) vs. Frequency from Carrier at 4.3 GHz, V_{CB} = 15 V, I_C = 30 mA.

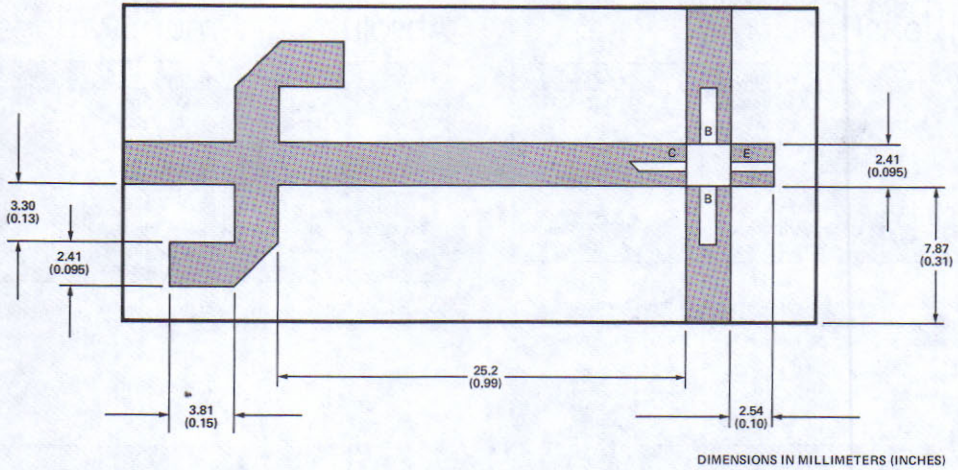


Figure 5. 4.3 GHz Oscillator Test Circuit.

Typical S-Parameters V_{CB} = 15 V, I_C = 30 mA

Freq. (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
1000	0.932	161	1.93	-29	0.011	127	1.017	-15
1500	0.943	153	1.92	-44	0.023	126	1.046	-31
2000	0.964	144	1.95	-59	0.039	120	1.068	-45
2500	0.986	134	1.97	-76	0.061	113	1.100	-59
3000	0.996	123	1.96	-94	0.086	105	1.120	-74
3500	1.015	115	1.95	-114	0.117	93	1.168	-91
4000	1.023	106	1.87	-133	0.154	84	1.193	-108
4500	1.014	96	1.79	-155	0.186	70	1.202	-127
5000	0.986	88	1.65	-174	0.217	58	1.215	-143
6000	0.914	74	1.32	144	0.245	35	1.103	-176
7000	0.857	61	1.06	109	0.267	17	0.996	157
8000	0.786	49	0.87	74	0.298	1	0.893	135
9000	0.760	44	0.76	60	0.238	-10	0.935	131
10000	0.725	27	0.72	29	0.288	-24	0.899	113
11000	0.702	6	0.68	5	0.302	-38	0.844	102
12000	0.645	-24	0.67	-25	0.320	-58	0.820	92

HEWLETT PACKARD

LINEAR POWER TRANSISTOR

2N6701 (HXTR-5101)

Bipolar Transistors

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz
22 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
13 dB Typical at 2 GHz
7.5 dB Typical at 4 GHz

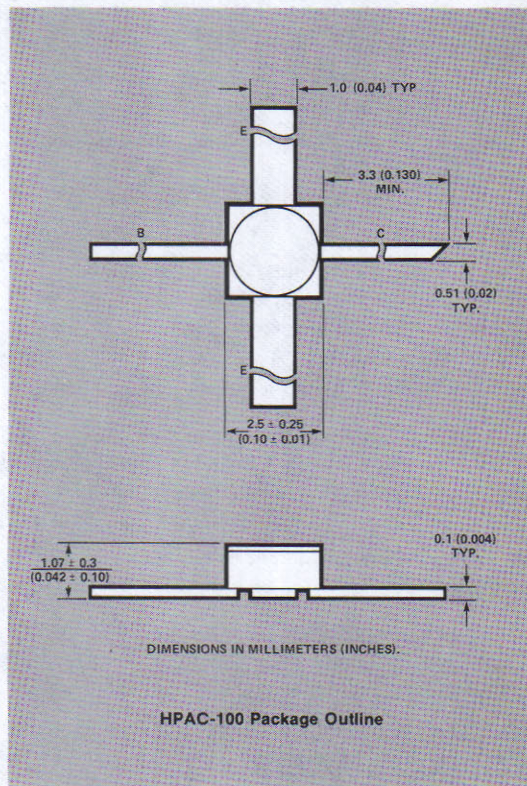
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

INFINITE SWR TOLERANCE ABOVE 2 GHz

RUGGED HERMETIC PACKAGE



HPAC-100 Package Outline

Description/Applications

The 2N6701 (HXTR-5101) is an NPN bipolar transistor designed for high output power and gain up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior gain, power, and distortion performance of the 2N6701 commend it for applications in radar, ECM, space, and commercial and military telecommunications. The 2N6701 features both guaranteed power output and associated gain at 1 dB gain compression.

The 2N6701 is supplied in the HPAC-100, a metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE} =25°C

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C = 3mA	3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C = 15mA	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B = 30μA	3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2V	3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32V	3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20V	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18V, I_C = 30mA	3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression f=2GHz		dBm		23	
	4GHz			21	22	
G_{1dB}	Associated 1dB Compressed Gain 2GHz		dB		13	
	4GHz			6.5	7.5	
P_{SAT}	Saturated Power Output (8dB Gain) 2GHz		dBm		25.5	
	(3dB Gain) 4GHz				25	
η	Power-Added Efficiency at 1dB Compression 2GHz		%		35	
	4GHz				24	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP) = 22dBm 4GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18V, I_C=30mA					

*300μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	24V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	50 mA
P_T	Total Device Dissipation[3]	700 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5×10^6 hours at T_J = 125°C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25°C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings *

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.1 W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

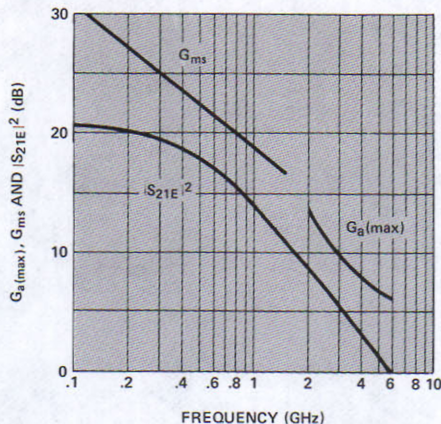


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), and $|S_{21E}|^2$ vs. Frequency at V_{CE} = 18V, I_C = 30mA.

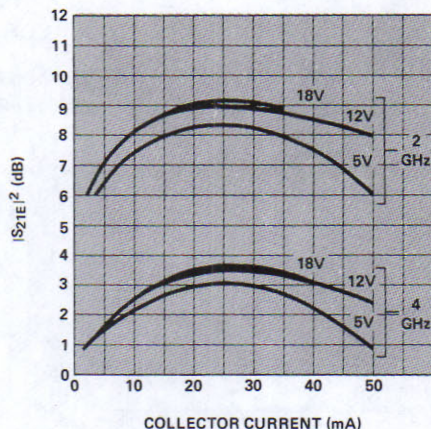


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 2 and 4 GHz.

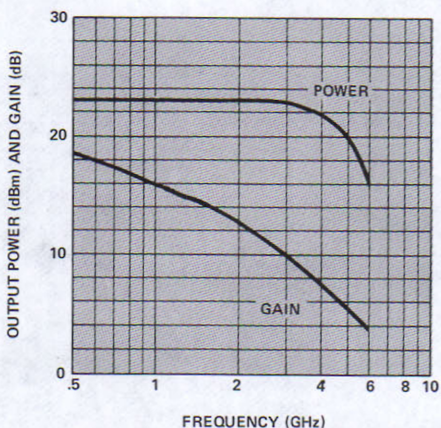


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 30mA.

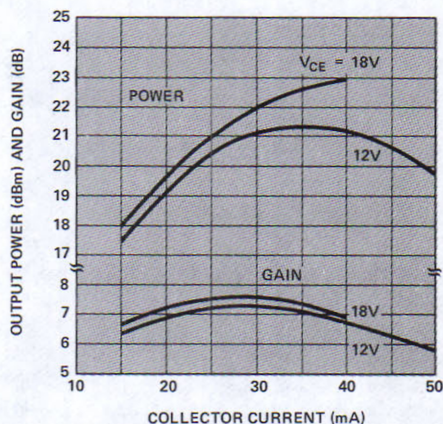


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

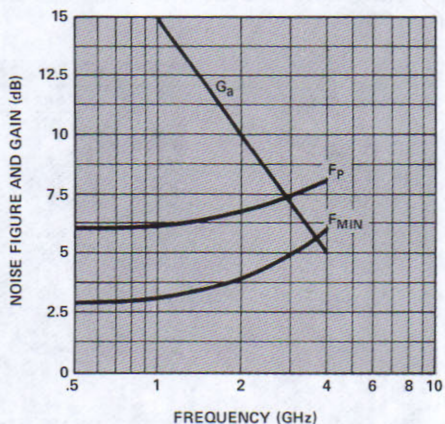


Figure 5. Typical Noise Figure (F_{min}) and Associated Gain (G_a) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 10mA. Typical Noise Figure (F_P) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 30mA.

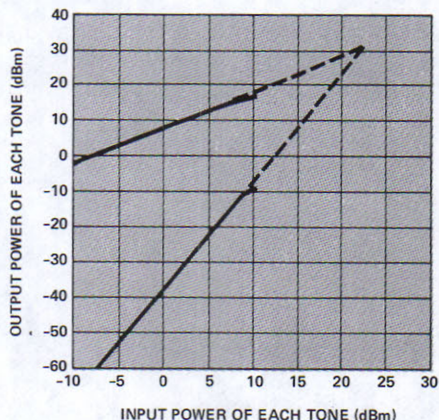


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 4GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 30mA.

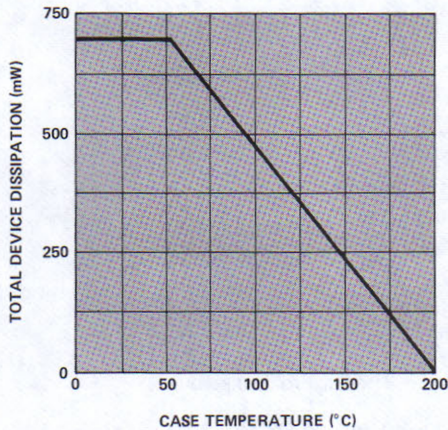


Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 210° C/W, T_{jMAX} = 200° C.

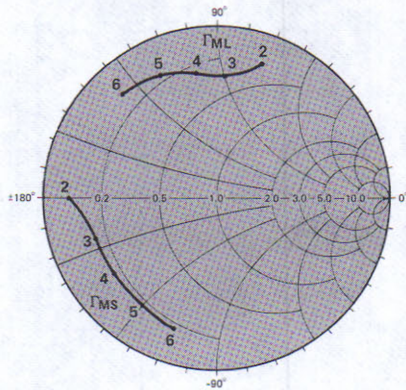


Figure 8. Typical Γ_{MS}, Γ_{ML}, (calculated from the average S-parameters) in the 2 to 6GHz frequency range, at V_{CE} = 18V, I_C = 30mA.

Typical S-Parameters V_{CE} = 18V, I_C = 30mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.80	-19	20.6	10.7	165	-37	0.01	77	0.98	-8
200	0.78	-37	20.1	10.2	154	-31	0.03	67	0.94	-15
300	0.75	-53	19.5	9.44	143	-28	0.04	60	0.88	-21
400	0.72	-68	18.7	8.63	133	-27	0.05	53	0.83	-26
500	0.68	-81	17.9	7.87	124	-26	0.05	47	0.78	-30
600	0.66	-92	17.0	7.15	117	-25	0.06	42	0.73	-33
700	0.64	-102	16.2	6.52	110	-24	0.06	39	0.69	-36
800	0.62	-111	15.5	5.96	104	-24	0.07	36	0.66	-38
900	0.61	-119	14.8	5.49	99	-23	0.07	33	0.64	-41
1000	0.60	-126	14.1	5.08	94	-23	0.07	31	0.61	-43
1500	0.56	-151	11.2	3.64	75	-23	0.08	25	0.55	-51
2000	0.55	-169	8.9	2.80	59	-22	0.08	22	0.52	-61
2500	0.56	179	7.2	2.29	45	-21	0.09	21	0.53	-72
3000	0.55	168	5.7	1.93	33	-21	0.09	21	0.52	-79
3500	0.56	158	4.5	1.69	21	-20	0.10	20	0.55	-89
4000	0.54	148	3.5	1.50	10	-19	0.11	19	0.58	-96
4500	0.54	137	2.5	1.33	0	-19	0.11	18	0.58	-106
5000	0.52	128	1.6	1.21	-11	-18	0.13	16	0.62	-113
5500	0.54	115	1.0	1.12	-23	-17	0.14	14	0.60	-122
6000	0.54	108	0.0	1.01	-32	-17	0.15	11	0.64	-132

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.80	-18	19.4	9.35	166	-37	0.01	78	0.98	-7
200	0.78	-35	19.1	9.07	155	-31	0.02	69	0.95	-14
300	0.76	-50	18.5	8.44	145	-28	0.03	61	0.91	-20
400	0.73	-64	17.8	7.79	135	-26	0.04	55	0.86	-25
500	0.69	-77	17.1	7.16	127	-25	0.05	49	0.81	-29
600	0.67	-88	16.3	6.56	119	-24	0.06	44	0.76	-32
700	0.64	-97	15.5	6.02	113	-23	0.06	40	0.72	-35
800	0.62	-107	14.8	5.54	107	-23	0.06	37	0.69	-38
900	0.60	-115	14.2	5.13	101	-23	0.07	34	0.66	-40
1000	0.60	-122	13.5	4.76	96	-23	0.07	32	0.63	-43
1500	0.57	-148	10.8	3.47	76	-22	0.08	24	0.57	-53
2000	0.55	-166	8.6	2.69	60	-21	0.08	21	0.54	-63
2500	0.56	-178	6.9	2.21	46	-21	0.09	19	0.55	-75
3000	0.56	171	5.1	1.80	36	-20	0.09	21	0.50	-85
3500	0.56	160	4.3	1.65	21	-20	0.10	18	0.56	-91
4000	0.53	151	3.3	1.47	10	-19	0.11	18	0.59	-99
4500	0.53	141	2.3	1.30	0	-19	0.11	17	0.59	-108
5000	0.50	130	1.5	1.18	-10	-18	0.12	15	0.62	-116
5500	0.52	118	0.8	1.10	-22	-17	0.14	13	0.61	-124
6000	0.53	110	0.0	0.99	-31	-16	0.15	11	0.64	-135

HEWLETT PACKARD

LINEAR POWER TRANSISTOR

HXTR-5102

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2 GHz
27.5 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
11.5 dB Typical at 2 GHz
7 dB Typical at 4 GHz

PARTIAL MATCHING FOR BROADBAND OPERATION

LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

INFINITE SWR TOLERANCE ABOVE 2 GHz

RUGGED HERMETIC PACKAGE

HPAC-200 GB/GT Package Outline

Description/Applications

The HXTR-5102 is an NPN bipolar transistor designed for high output power and gain up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness. A silicone conformal coating protects the chip and matching network.

The superior power, gain and distortion performance of the HXTR-5102 commend it for use in broad and narrowband commercial and military telecommunications, radar and ECM applications. Additionally, its partial internal matching makes it ideal for broad bandwidth designs in the 2 to 5 GHz frequency range with minimal sacrifice of output power and gain.

The HXTR-5102 is supplied in the HPAC-200GB/GT, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE} =25°C

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C=10 mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C=50 mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B=100 μA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2 V		3061.1	μA			5
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32 V		3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20 V		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18 V, I_C=110 mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f=2 GHz		dBm		29	
		4 GHz			26.5	27.5	
G_{1dB}	Associated 1dB Compressed Gain	2 GHz		dB		11.5	
		4 GHz			6.0	7.0	
P_{SAT}	Saturated Power Output (8 dB Gain)	2 GHz		dBm		31.0	
	(3 dB Gain)	4 GHz				29.5	
η	Power-Added Efficiency at 1 dB Compression	2 GHz		%		37	
		4 GHz				23	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP)=.5 W	4 GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18 V, I_C=110 mA						

*300 μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	22V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	150 mA
P_T	Total Device Dissipation[3]	2.7 W
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125°C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25°C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

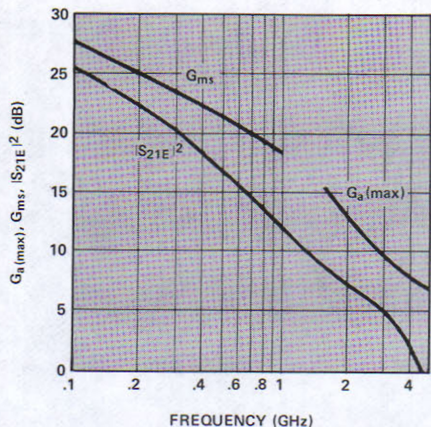


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), and $|S_{21E}|^2$ vs. Frequency at V_{CE} = 18V, I_C = 110mA.

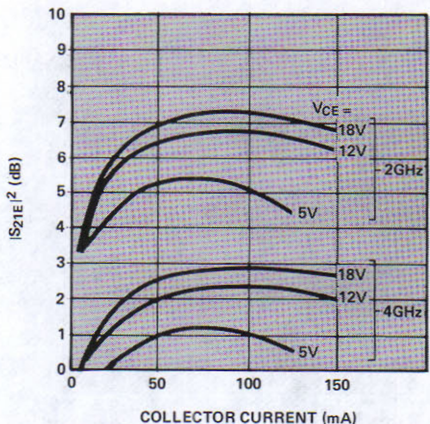


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 2 and 4 GHz.

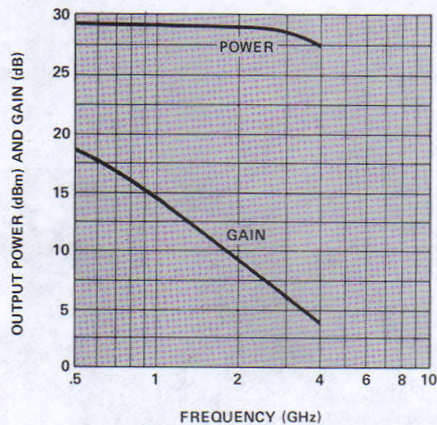


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 110mA.

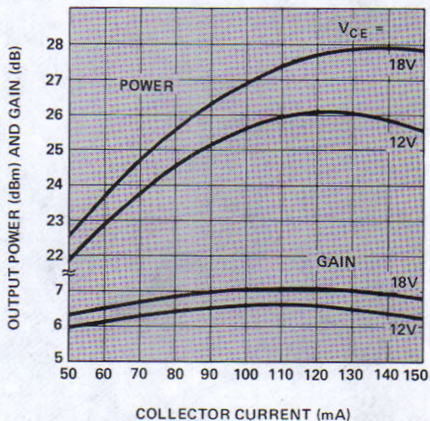


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4 GHz.

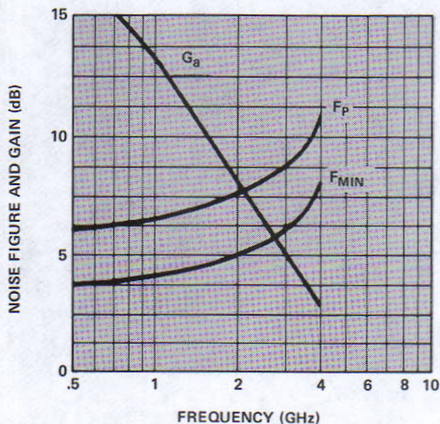


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 25mA. Typical Noise Figure (F_p) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 110mA.

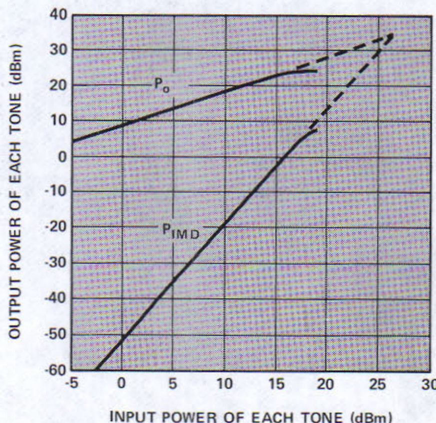


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 4GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 110mA.

Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 55°C/W, T_{jMAX} = 200°C.

Figure 8. Typical Γ_{MS}, Γ_{ML} (calculated from the average S-parameters) in the 2 to 5.5GHz frequency range, for V_{CE} = 18V, I_C = 110mA.

Typical S-Parameters V_{CE} = 18 V, I_C = 110 mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang
100	0.55	-74	25.4	18.6	146	-31	0.03	56	0.85	-29
200	0.65	-109	22.7	13.6	123	-28	0.04	39	0.68	-47
300	0.70	-134	20.8	10.9	108	-27	0.05	28	0.55	-59
400	0.72	-144	18.6	8.47	97	-26	0.05	21	0.48	-65
500	0.74	-158	17.2	7.22	88	-26	0.05	17	0.42	-74
600	0.73	-160	15.6	5.99	81	-25	0.05	13	0.41	-75
700	0.74	-167	14.6	5.39	76	-25	0.05	11	0.39	-79
800	0.74	-170	13.4	4.66	69	-25	0.06	8	0.39	-82
900	0.74	-175	12.7	4.32	64	-25	0.06	8	0.38	-86
1000	0.74	-178	11.8	3.91	59	-25	0.06	7	0.37	-92
1500	0.71	166	9.0	2.82	34	-24	0.06	-2	0.43	-107
2000	0.64	153	7.3	2.32	10	-23	0.07	-8	0.51	-119
2500	0.52	140	6.3	2.07	-17	-22	0.08	-22	0.61	-133
3000	0.32	129	5.4	1.86	-49	-21	0.09	-42	0.73	-148
3500	0.15	158	3.8	1.55	-83	-20	0.09	-67	0.77	-165
4000	0.32	-145	2.8	1.38	-113	-22	0.08	-98	0.80	-177
4500	0.52	-158	0.0	1.00	-142	-24	0.06	132	0.82	171
5000	0.70	176	-1.9	0.81	-170	-28	0.04	50	0.87	159
5500	0.78	155	-3.0	0.71	161	-28	0.04	85	0.83	142
6000	0.85	119	-3.9	0.64	121	-19	0.11	16	0.93	121

HEWLETT PACKARD

LINEAR POWER TRANSISTOR

2N6741 (HXTR-5103)

Bipolar Transistors

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz

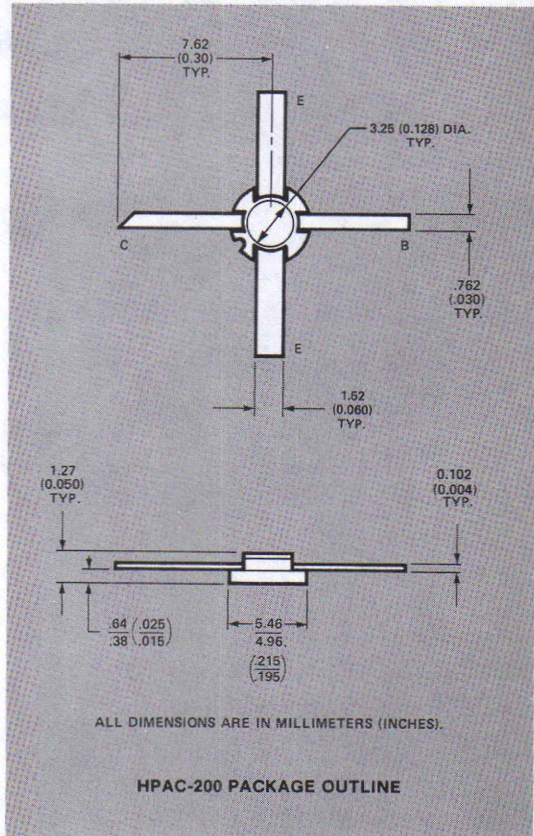
HIGH P_{1dB} GAIN
11 dB Typical at 2 GHz

LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

RUGGED HERMETIC PACKAGE



HPAC-200 PACKAGE OUTLINE

Description/Applications

The HXTR-5103 is an NPN bipolar transistor designed for high gain and linear output power up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques, and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5103 commend it for use in RF and IF applications in radar, ECM, space, and other commercial and military communications.

The HXTR-5103 utilizes the HPAC-200, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE}=25°C$

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C=3mA$		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C=15mA$		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B=30\mu A$		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB}=2V$		3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at $V_{CE}=32V$		3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB}=20V$		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=18V$, $I_C=30mA$		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f= 2GHz		dBm	22	23	
G_{1dB}	Associated 1dB Compressed Gain	2GHz		dB	9.5	11	
P_{SAT}	Saturated Power Output (Gain=5dB)	2GHz		dBm		25	
η	Power-Added Efficiency at 1dB Compression	2GHz		%		34	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at Po(PEP)=.2W	2GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE}=18V$, $I_C=30mA$						

*300μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	24V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	50 mA
P_T	Total Device Dissipation[3]	700 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4.0V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.4 W
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

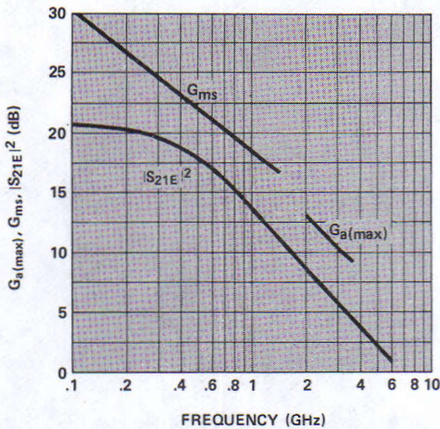


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), and $|S_{21E}|^2$ vs. Frequency at $V_{CE} = 18V$, $I_C = 30mA$.

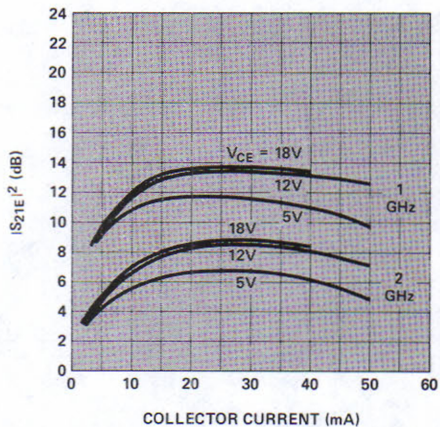


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1 and 2GHz.

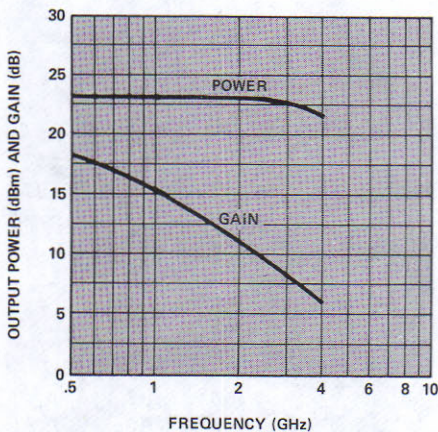


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at $V_{CE} = 18V$, $I_C = 30mA$.

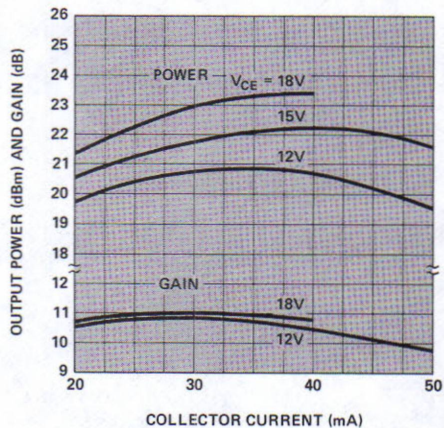


Figure 4. Typical P_{1dB} Linear Output Power and Associated 1dB Compressed Gain vs. Current at 2 GHz.

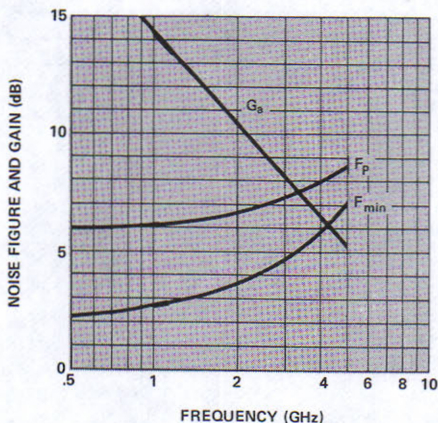


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) vs. Frequency when tuned for Minimum Noise at $V_{CE} = 18V$, $I_C = 10mA$. Typical Noise Figure (F_p) when tuned for Max P_{1dB} at $V_{CE} = 18V$, $I_C = 30mA$.

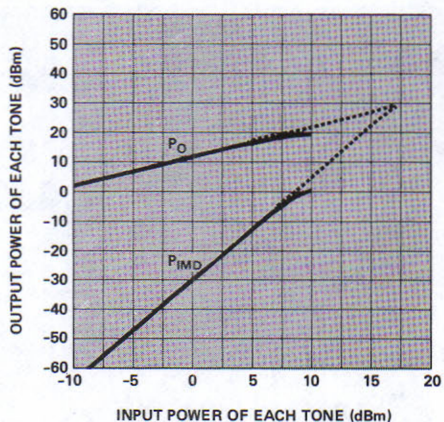


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 2GHz for a frequency separation of 5MHz at $V_{CE} = 18V$, $I_C = 30mA$.

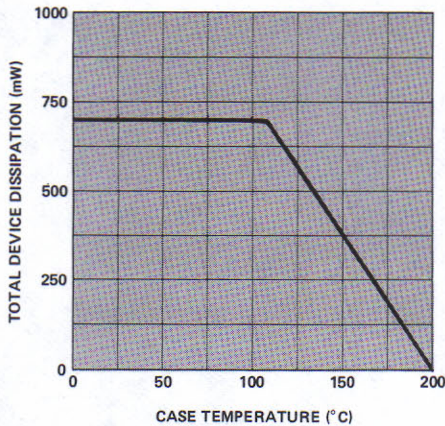


Figure 7. Power Dissipation Curve for θ_{jc} = 125°C/W, T_{JMAX} = 200°C.

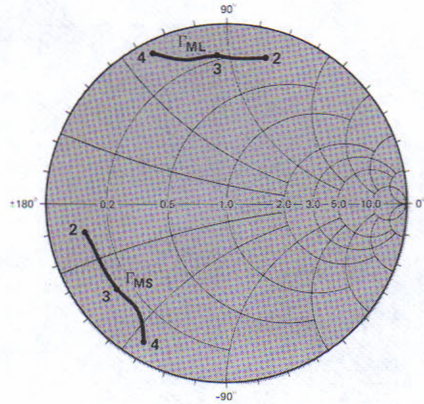


Figure 8. Typical Γ_{MS}, Γ_{ML} (Calculated from the Average S-Parameters) in the 2 to 4GHz Frequency Range for V_{CE} = 18V, I_C = 30mA.

Typical S-Parameters V_{CE} = 18V, I_C = 30mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.74	-20	20.7	10.9	165	-37	0.01	79	0.98	-9
200	0.71	-40	20.3	10.3	152	-32	0.03	68	0.94	-17
300	0.68	-57	19.6	9.49	140	-29	0.04	62	0.89	-23
400	0.65	-72	18.7	8.65	130	-27	0.04	55	0.84	-28
500	0.62	-86	17.8	7.77	121	-26	0.05	49	0.79	-33
600	0.60	-97	16.9	7.01	113	-25	0.06	44	0.75	-37
700	0.58	-108	16.2	6.43	106	-25	0.06	41	0.71	-40
800	0.55	-116	15.4	5.87	100	-24	0.06	38	0.68	-42
900	0.54	-124	14.6	5.38	94	-24	0.07	35	0.65	-44
1000	0.52	-131	13.8	4.91	88	-23	0.07	33	0.63	-46
1500	0.49	-159	11.0	3.53	66	-22	0.08	25	0.58	-59
2000	0.47	-179	8.8	2.77	48	-21	0.09	22	0.56	-67
2500	0.47	165	7.1	2.27	32	-20	0.10	18	0.56	-81
3000	0.45	151	5.8	1.95	17	-19	0.11	15	0.59	-90
3500	0.45	138	4.7	1.71	2	-18	0.12	10	0.59	-103
4000	0.42	123	3.7	1.54	-11	-17	0.14	4	0.64	-111
4500	0.41	110	3.2	1.44	-24	-16	0.16	1	0.65	-121
5000	0.39	89	2.2	1.29	-38	-15	0.17	-6	0.69	-131
5500	0.39	74	1.4	1.18	-53	-14	0.19	-12	0.69	-139
6000	0.37	55	0.7	1.09	-64	-13	0.22	-17	0.69	-148

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.74	-19	19.1	9.05	164	-37	0.01	81	0.98	-8
200	0.70	-37	18.8	8.76	152	-31	0.03	68	0.94	-15
300	0.67	-54	18.2	8.16	141	-28	0.04	60	0.90	-21
400	0.63	-69	17.5	7.52	130	-27	0.05	53	0.85	-26
500	0.60	-83	16.8	6.90	121	-26	0.05	48	0.80	-31
600	0.58	-95	16.0	6.32	113	-25	0.06	43	0.76	-35
700	0.57	-105	15.2	5.78	107	-24	0.06	40	0.73	-38
800	0.55	-113	14.5	5.29	101	-24	0.07	37	0.70	-40
900	0.54	-121	13.8	4.88	95	-23	0.07	34	0.67	-43
1000	0.52	-128	13.0	4.48	89	-23	0.07	31	0.65	-45
1500	0.48	-156	10.2	3.23	66	-22	0.08	25	0.60	-55
2000	0.46	-177	8.0	2.51	48	-21	0.09	21	0.56	-65
2500	0.46	167	6.3	2.00	31	-20	0.10	18	0.57	-77
3000	0.45	153	5.0	1.78	16	-19	0.11	16	0.59	-86
3500	0.44	140	3.8	1.56	0	-18	0.12	12	0.60	-98
4000	0.43	126	2.8	1.38	-13	-17	0.14	8	0.64	-106
4500	0.41	112	1.9	1.24	-26	-16	0.15	4	0.64	-114
5000	0.38	93	1.0	1.12	-40	-15	0.17	-1	0.68	-123
5500	0.39	74	0.8	1.09	-55	-14	0.20	-6	0.70	-130
6000	0.37	56	-0.3	0.96	-67	-13	0.23	-12	0.69	-139

HEWLETT PACKARD

LINEAR POWER TRANSISTOR

HXTR-5104

Bipolar Transistors

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2 GHz

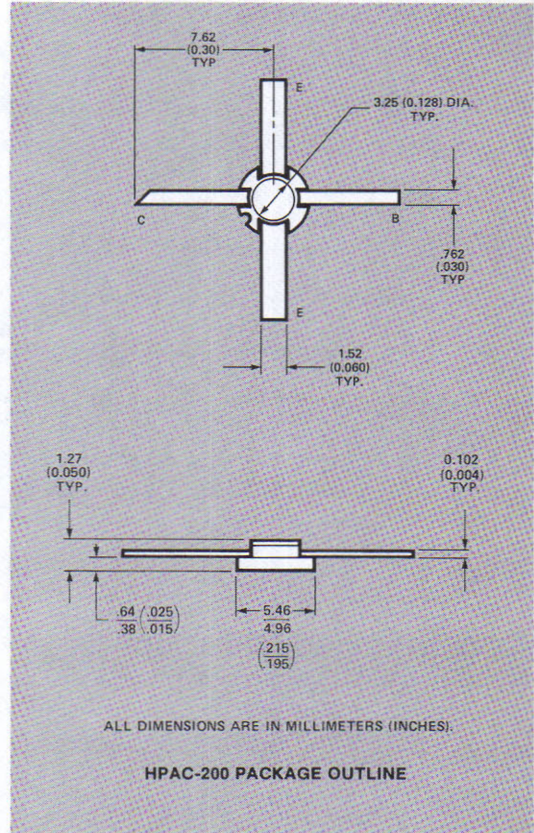
HIGH P_{1dB} GAIN
9 dB Typical at 2 GHz

LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

RUGGED HERMETIC PACKAGE



ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPAC-200 PACKAGE OUTLINE

Description/Applications

The HXTR-5104 is an NPN bipolar transistor designed for high gain and linear output power up to 4 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques, and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5104 commend it for use in RF and IF applications in radar, ECM, space, and other commercial and military communications.

The HXTR-5104 utilizes the HPAC-200, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE}=25°C$

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C=10mA$	3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C=50mA$	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B=100\mu A$	3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB}=2V$	3061.1	µA			10
I_{CES}	Collector-Emitter Leakage Current at $V_{CE}=32V$	3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB}=20V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=18V$, $I_C=110mA$	3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression f= 2GHz		dBm	28	29	
G_{1dB}	Associated 1dB Compressed Gain 2GHz		dB	8	9	
P_{SAT}	Saturated Power Output (Gain=5dB) 2GHz		dBm		31	
η	Power-Added Efficiency at 1dB Compression 2GHz		%		35	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at $P_O(PEP)=0.7W$ 2GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE}=18V$, $I_C=110mA$					

*300µs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage(2)	40V
V_{CEO}	Collector to Emitter Voltage(2)	22V
V_{EBO}	Emitter to Base Voltage(2)	3.3V
I_C	DC Collector Current(2)	150 mA
P_T	Total Device Dissipation(3)	2.7 W
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125°C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25°C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4 W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

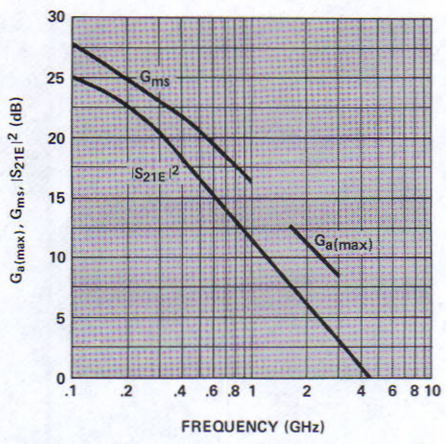


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), and $|S_{21E}|^2$ vs. Frequency at V_{CE} = 18V, I_C = 110mA.

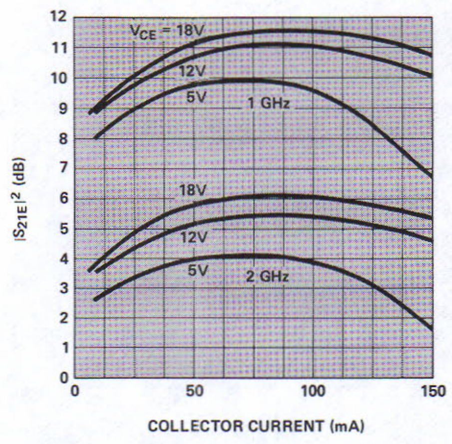


Figure 2. Typical $|S_{21E}|^2$ vs. Current at 1 and 2GHz.

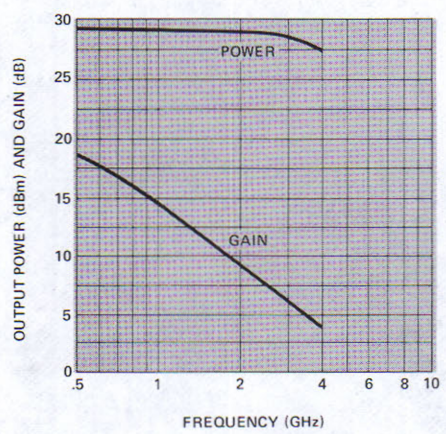


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 110mA.

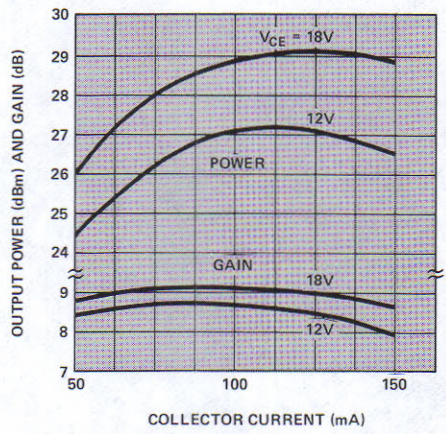


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 2 GHz.

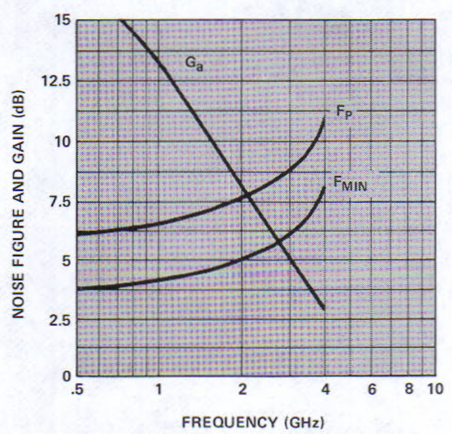


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 25mA. Typical Noise Figure (F_p) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 110mA.

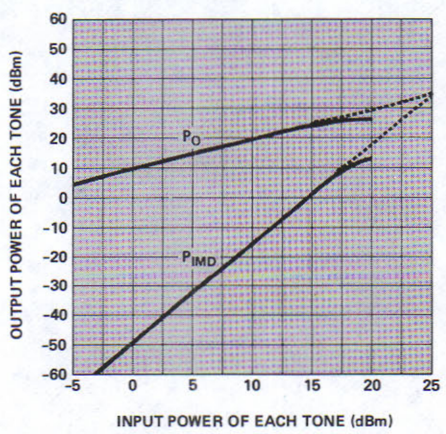


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 2GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 110mA.

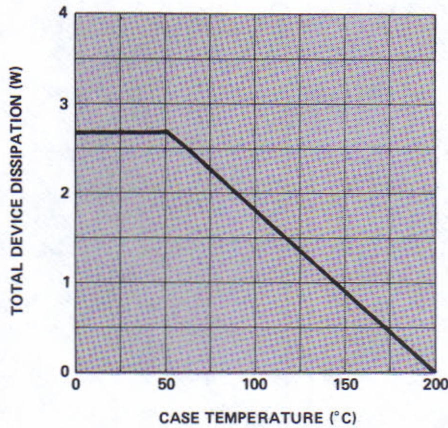


Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 55°C/W, T_{jMAX} = 200°C.

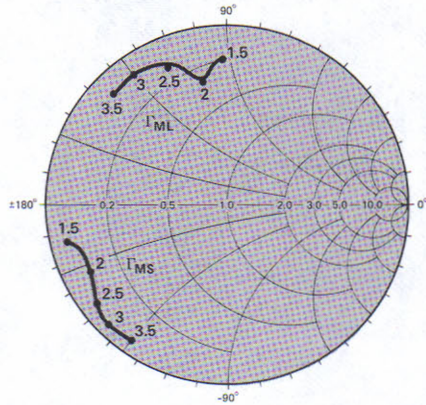
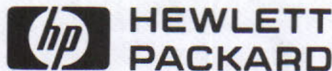


Figure 8. Typical Γ_{MS}, Γ_{ML} (calculated from the average S-parameters) in the 1.5 to 3.5GHz frequency range, at V_{CE} = 18V, I_C = 110mA.

Typical S-Parameters V_{CE} = 18V, I_C = 110mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.48	-68	24.8	17.3	140	-31	0.03	62	0.86	-27
200	0.54	-109	22.6	13.5	127	-27	0.04	48	0.69	-46
300	0.59	-132	20.4	10.5	112	-26	0.05	40	0.55	-58
400	0.61	-146	18.5	8.43	102	-25	0.06	36	0.47	-66
500	0.63	-155	16.9	7.02	94	-24	0.06	34	0.41	-71
600	0.64	-162	15.5	5.98	88	-24	0.06	33	0.38	-76
700	0.65	-168	14.3	5.21	83	-24	0.07	33	0.35	-80
800	0.65	-172	13.3	4.62	78	-23	0.07	33	0.34	-84
900	0.65	-176	12.4	4.15	73	-23	0.07	33	0.32	-87
1000	0.64	179	11.5	3.70	69	-22	0.08	32	0.32	-90
1500	0.65	169	8.2	2.57	50	-20	0.10	31	0.32	-104
2000	0.65	151	6.0	1.99	33	-19	0.11	30	0.33	-118
2500	0.66	139	4.3	1.64	17	-17	0.14	25	0.39	-130
3000	0.65	128	2.9	1.40	2	-16	0.16	20	0.42	-140
3500	0.64	115	1.8	1.23	-13	-15	0.19	14	0.46	-152
4000	0.63	103	0.9	1.11	-27	-13	0.22	5	0.51	-161
4500	0.61	87	0.2	1.03	-41	-12	0.26	-2	0.53	-172
5000	0.59	72	-0.7	0.93	-54	-11	0.29	-12	0.57	179
5500	0.58	53	-1.6	0.84	-67	-10	0.34	-22	0.57	167
6000	0.58	38	-2.3	0.77	-79	-9	0.37	-31	0.60	155



LOW NOISE TRANSISTOR

2N6617
(HXTR-6101)
2N6742
(HXTR-6102)

Bipolar Transistors

Features

LOW NOISE FIGURE
2.8dB at 4GHz, Typical (2N6617)
2.5dB at 4GHz, Typical (2N6742)

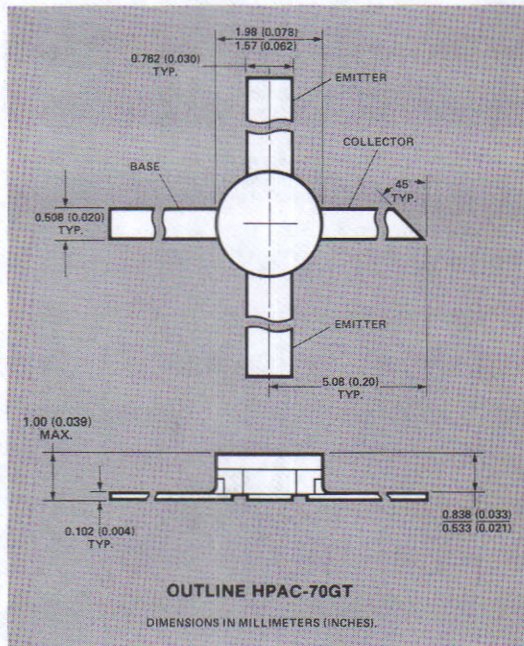
HIGH GAIN
9.0dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction

Description

The 2N6617 (HXTR-6101) and 2N6742 (HXTR-6102) are NPN bipolar transistors designed for minimum noise figure at 4GHz. These devices utilize ion implantation techniques in their manufacture and the chip is also provided with scratch protection over its active area. These devices are supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

The HXTR-6102 is a lower noise selection of the 2N6617.



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C=100\mu A$	3001.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE}=10V$	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB}=10V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=10V$, $I_C=4mA$	3076.1*	–	50	150	250
F_{MIN}	Minimum Noise Figure f = 1.5 GHz (2N6617) 4 GHz (2N6617) 4 GHz (2N6742)	3246.1	dB		1.6 2.8 2.5	 3.0 2.7
G_a	Associated Gain f = 1.5 GHz (2N6617) 4 GHz (2N6617/2N6742) Bias Conditions for Above: $V_{CE} = 10V$, $I_C = 4mA$		dB dB	 8.0	15 9.0	
M_{MIN}**	Minimum Noise Measure (2N6617) $V_{CE} = 10V$, $I_C = mA$, f = 4GHz (2N6742)				3.1 2.8	3.4 3.1

*300µs wide pulse measurement at ≤2% duty cycle.

**$M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 4 mW/° C, $T_C \geq$ 163° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

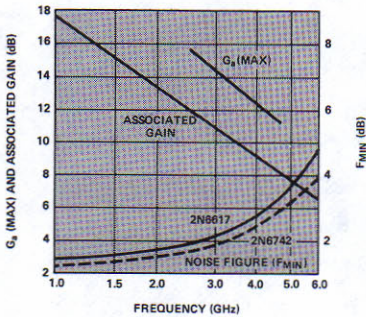


Figure 1. Typical $G_{a(MAX)}$, F_{MIN} and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 4 mA.

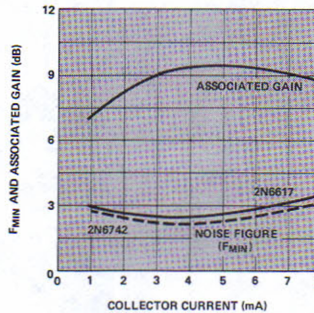


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 4 GHz for V_{CE} = 10V (Tuned for F_{MIN}).

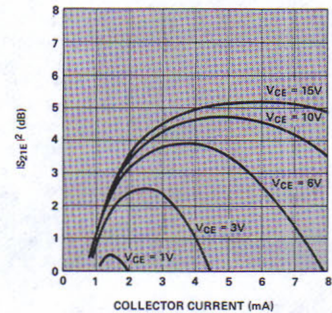


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 4 GHz, for the 2N6617/2N6742.

Typical S-Parameters V_{CE} = 10V, I_C = 4mA

Freq. (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
100	0.917	-11	7.149	168	0.007	79	0.991	-4
500	0.782	-54	6.277	135	0.026	54	0.901	-18
1000	0.635	-98	5.037	113	0.037	33	0.787	-30
1500	0.598	-127	3.881	87	0.039	28	0.763	-35
2000	0.589	-149	3.148	71	0.042	26	0.754	-43
2500	0.570	-163	2.646	59	0.042	25	0.760	-50
3000	0.575	-173	2.209	48	0.043	25	0.773	-58
3500	0.560	180	1.948	37	0.046	25	0.795	-64
4000	0.548	173	1.665	29	0.049	24	0.816	-71
4500	0.530	167	1.450	20	0.053	24	0.850	-76
5000	0.518	160	1.346	11	0.058	23	0.860	-84
5500	0.500	152	1.210	1	0.060	22	0.880	-92
6000	0.489	146	1.076	-7	0.063	20	0.877	-99
7000	0.491	132	0.897	-23	0.069	15	0.872	-108

Bipolar Transistors

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB) 2N6742	2N6617
1000	.480/23°	23.31	1.20	1.45
1500	.450/61°	15.57	1.39	1.58
2000	.410/88°	15.73	1.57	1.72
3000	.425/121°	10.72	1.85	2.18
4000	.475/166°	3.50	2.48	2.75
5000	.530/-164°	2.81	3.20	3.67
6000	.520/-131°	7.23	3.95	4.78

Figure 4. Typical Noise Parameters for the 2N6742/2N6617 at V_{CE} = 10V, I_C = 4 mA.

Low Power Bias Performance

Bias V_{CE} V	I_C mA	F_{MIN} dB	G_a dB	R_N Ohms	Γ_o Mag./Ang.	Γ_L Mag./Ang.
3	0.25	2.25	8.5	60.5	.805/31°	.788/25°
3	0.50	1.87	12.7	25.5	.713/38°	.779/29°
3	1.00	1.55	15.7	13.9	.571/39°	.774/29°

Figure 5. Noise Parameters at 1 GHz for the 2N6617 (HXTR-6101)

BIAS		Frequency 1000 MHz		1500 MHz		2000 MHz		3000MHz	
V_{CE} V	I_C mA	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB
3	0.25	2.25	8.5	2.67	5.0	2.83	4.7	3.88	4.1
3	0.50	1.87	12.7	2.06	9.9	2.23	7.9	2.93	6.4
3	1.0	1.55	15.7	1.73	11.7	1.79	10.2	2.38	8.1

Figure 6. Noise Performance vs. Frequency and Bias for the 2N6617 (HXTR-6101)

TYPICAL S-PARAMETERS V_{CE} = 3V, I_C = 0.25mA

Freq. (MHz)	S_{11} Mag.	Ang.	S_{21} (dB)	Mag.	Ang.	S_{12} (dB)	Mag.	Ang.	S_{22} Mag.	Ang	K
500	.988	-22	-6.9	.451	152	-28.2	.039	72	.993	-12	.220
1000	.956	-42	-7.2	.438	127	-23.1	.070	55	.975	-22	.464
1500	.929	-65	-7.5	.423	106	-20.6	.093	38	.956	-33	.586
2000	.910	-81	-7.7	.412	89	-19.7	.104	27	.945	-42	.679
3000	.888	-112	-8.1	.394	56	-19.3	.108	6	.938	-59	.821

V_{CE} = 3V, I_C = 0.50mA

Freq. (MHz)	S_{11} Mag.	Ang.	S_{21} (dB)	Mag.	Ang.	S_{12} (dB)	Mag.	Ang.	S_{22} Mag.	Ang.	K
500	.976	-24	-0.8	.991	152	-28.4	.038	70	.986	-13	.220
1000	.929	-47	-1.3	.863	128	-23.6	.066	52	.955	-24	.423
1500	.887	-72	-2.0	.792	107	-21.4	.085	35	.920	-34	.583
2000	.856	-89	-2.5	.747	91	-20.6	.093	24	.906	-43	.682
3000	.818	-121	-3.3	.688	60	-20.1	.099	7	.889	-60	.816

V_{CE} = 3V, I_C = 1.0mA

Freq. (MHz)	S_{11} Mag.	Ang.	S_{21} (dB)	Mag.	Ang.	S_{12} (dB)	Mag.	Ang.	S_{22} Mag.	Ang.	K
500	.952	-25	4.4	1.67	149	-28.6	.037	66	.972	-14	.328
1000	.884	-54	3.7	1.54	125	-24.3	.061	47	.919	-25	.492
1500	.821	-82	2.7	1.36	104	-23.1	.070	31	.873	-36	.664
2000	.775	-102	1.9	1.25	88	-22.6	.074	23	.854	-43	.793
3000	.738	-133	.77	1.09	59	-22.1	.079	10	.842	-59	.908

HEWLETT PACKARD

LOW NOISE TRANSISTOR

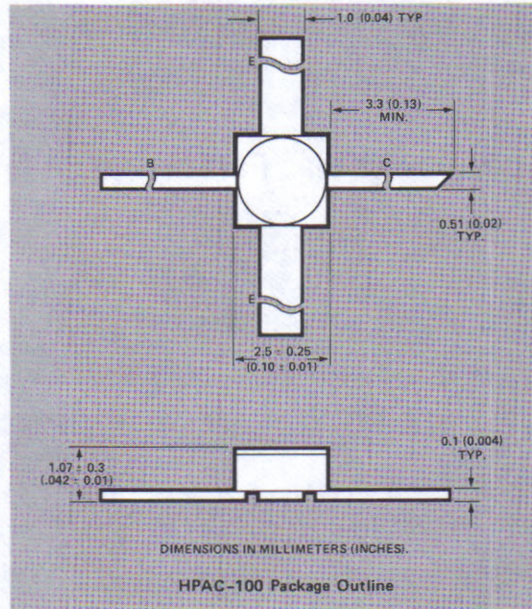
2N6618 (HXTR-6103)

Features

GUARANTEED LOW NOISE FIGURE
2.2 dB Max. at 2 GHz, 1.8 dB Typical

HIGH GAIN
12.0 dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction



HPAC-100 Package Outline

Description

The 2N6618 (HXTR-6103) is an NPN bipolar transistor designed for minimum noise figure at 2 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with scratch protection over its active area.

These devices are supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and are capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector Emitter Breakdown Voltage at $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector Emitter Leakage Current at $V_{CE} = 10V$	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at $V_{CB} = 10V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=10V, I_C=3mA$	3076.1*	—	50	150	250
F_{MIN}	Minimum Noise Figure at 2 GHz	3246.1	dB		1.8	2.2
G_a	Associated Gain at 2 GHz Bias for above: $V_{CE} = 10V, I_C = 3$ mA		dB	11.0	12.0	
M_{MIN}**	Minimum Noise Measure $V_{CE} = 10V, I_C = 3$ mA, f = 2 GHz				1.90	2.35

*300 μs wide pulse measurement at ≤ 2% duty cycle.

** $M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5 x 10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 3.3 mW/° C, $T_C \geq$ 155° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

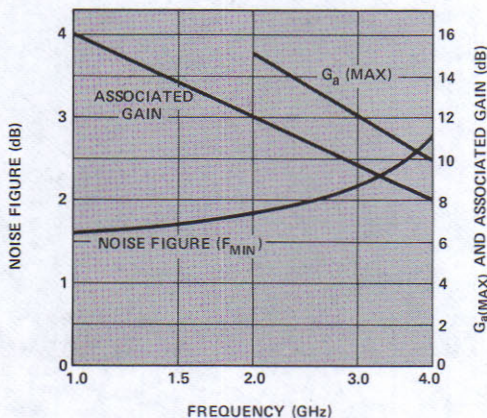


Figure 1. Typical $G_{a(max)}$, F_{MIN} and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 3 mA.

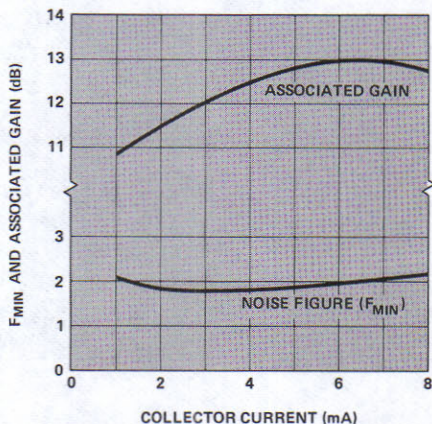


Figure 2. Typical F_{MIN} and Associated Gain vs. Collector Current at 2 GHz for V_{CE} = 10V (Tuned for F_{MIN}).

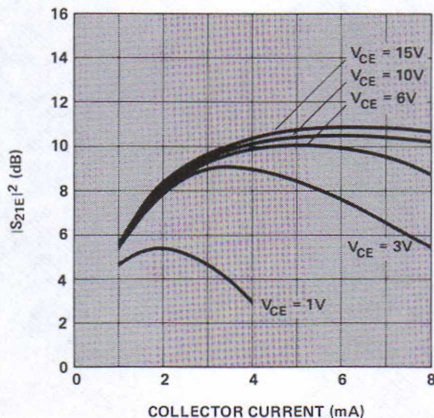


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 2 GHz.

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.465/36°	25.09	1.55
1500	.369/67°	22.47	1.65
2000	.323/94°	23.31	1.80

Figure 4. Typical Noise Parameters at V_{CE} = 10V, I_C = 3 mA.

Typical S-Parameters V_{CE} = 10V, I_C = 3 mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.93	-11.5	16.2	6.46	168.0	-42.0	0.01	77.0	0.99	-4.0
200	0.89	-23.0	17.1	7.13	158.0	-37.0	0.01	77.0	0.97	-8.0
300	0.86	-34.0	16.4	6.58	149.0	-34.0	0.02	66.0	0.94	-12.0
400	0.83	-44.0	15.9	6.26	142.0	-32.0	0.03	60.0	0.92	-16.0
500	0.79	-54.0	15.6	6.02	135.0	-30.0	0.03	55.0	0.89	-19.0
600	0.75	-65.0	15.4	5.91	128.0	-29.0	0.04	51.0	0.87	-21.0
700	0.71	-73.0	15.0	5.62	121.0	-29.0	0.04	48.0	0.85	-24.0
800	0.68	-81.0	14.4	5.25	116.0	-28.0	0.04	45.0	0.84	-25.0
900	0.65	-91.0	14.0	4.99	111.0	-28.0	0.04	43.0	0.83	-27.0
1000	0.62	-97.0	13.5	4.72	106.0	-27.0	0.04	41.0	0.81	-28.0
1500	0.52	-129.0	11.4	3.71	84.0	-27.0	0.05	32.0	0.74	-35.0
2000	0.50	-151.0	9.3	2.93	69.0	-26.0	0.05	31.0	0.72	-43.0
2500	0.50	-169.0	7.8	2.45	55.0	-26.0	0.05	31.0	0.69	-51.0
3000	0.49	175.0	6.5	2.12	42.0	-26.0	0.06	33.0	0.68	-57.0
3500	0.54	165.0	5.4	1.87	29.0	-25.0	0.06	35.0	0.65	-68.0
4000	0.52	156.0	4.5	1.67	19.0	-24.0	0.06	37.0	0.68	-76.0
5000	0.53	140.0	2.6	1.35	-3.0	-23.0	0.08	35.0	0.71	-96.0
6000	0.48	120.0	0.9	1.11	-22.0	-21.0	0.09	34.0	0.73	-112.0

HEWLETT PACKARD

LOW NOISE TRANSISTOR

2N6743 (HXTR-6104)

Bipolar Transistors

Features

GUARANTEED LOW NOISE FIGURE
1.6 dB Max. at 1.5 GHz

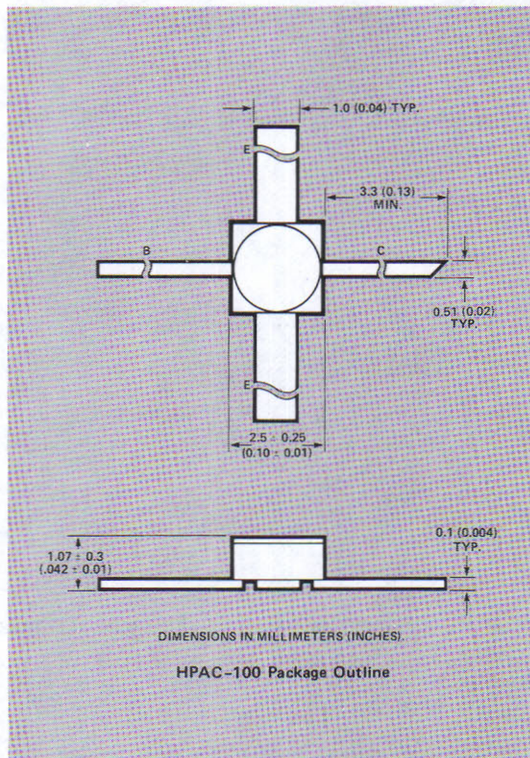
HIGH GAIN
14.0 dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction

Description

The 2N6743 (HXTR-6104) is an NPN bipolar transistor designed for minimum noise figure at 1.5 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with scratch protection over its active area.

The 2N6743 (HXTR-6104) is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.



HPAC-100 Package Outline

Typical Noise Parameters

at V_{CE} = 10V, I_C = 3 mA.

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.465/36°	25.09	1.20
1500	.369/67°	22.47	1.40
2000	.323/94°	23.31	1.50

Electrical Specifications at T_{CASE} = 25°C

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector Emitter Breakdown Voltage at I_C = 100μA	3011.1*	V	30		
I_{CEO}	Collector Emitter Leakage Current at V_{CE} = 10V	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at V_{CB} = 10V	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=10V, I_C=3mA	3076.1*	–	50	150	250
F_{MIN}	Minimum Noise Figure f = 1.5 GHz	3246.1	dB		1.4	1.6
G_a	Associated Gain f = 1.5 GHz Bias for above: V_{CE} = 10V, I_C = 3 mA		dB	13.0	14.0	
M_{MIN}**	Minimum Noise Measure V_{CE} = 10V, I_C = 3 mA, f = 1.5 GHz				1.45	1.67

*300 μs wide pulse measurement at ≤ 2% duty cycle.

**$M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5×10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 3.3 mW/° C, $T_C \geq 155°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

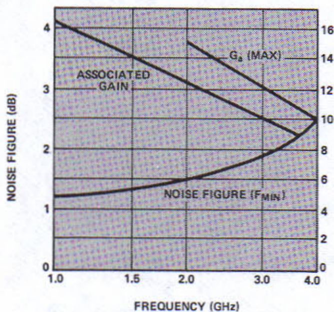


Figure 1. Typical $G_{a(max)}$, F_{MIN} and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 3 mA.

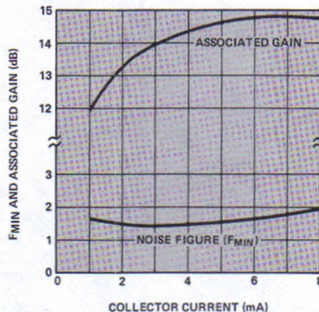


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 1.5 GHz for V_{CE} = 10V (Tuned for F_{MIN}).

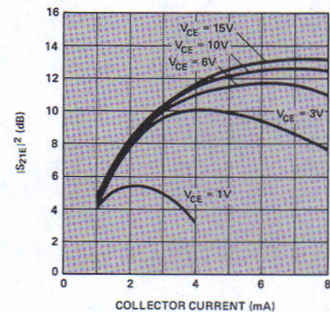


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 1.5 GHz.

Typical S-Parameters V_{CE} = 10V, I_C = 3 mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.93	-11.5	16.2	6.46	168.0	-42.0	0.01	77.0	0.99	-4.0
200	0.89	-23.0	17.1	7.13	158.0	-37.0	0.01	77.0	0.97	-8.0
300	0.86	-34.0	16.4	6.58	149.0	-34.0	0.02	66.0	0.94	-12.0
400	0.83	-44.0	15.9	6.26	142.0	-32.0	0.03	60.0	0.92	-16.0
500	0.79	-54.0	15.6	6.02	135.0	-30.0	0.03	55.0	0.89	-19.0
600	0.75	-65.0	15.4	5.91	128.0	-29.0	0.04	51.0	0.87	-21.0
700	0.71	-73.0	15.0	5.62	121.0	-29.0	0.04	48.0	0.85	-24.0
800	0.68	-81.0	14.4	5.25	116.0	-28.0	0.04	45.0	0.84	-25.0
900	0.65	-91.0	14.0	4.99	111.0	-28.0	0.04	43.0	0.83	-27.0
1000	0.62	-97.0	13.5	4.72	106.0	-27.0	0.04	41.0	0.81	-28.0
1500	0.52	-129.0	11.4	3.71	84.0	-27.0	0.05	32.0	0.74	-35.0
2000	0.50	-151.0	9.3	2.93	69.0	-26.0	0.05	31.0	0.72	-43.0
2500	0.50	-169.0	7.8	2.45	55.0	-26.0	0.05	31.0	0.69	-51.0
3000	0.49	175.0	6.5	2.12	42.0	-26.0	0.06	33.0	0.68	-57.0
3500	0.54	165.0	5.4	1.87	29.0	-25.0	0.06	35.0	0.65	-68.0
4000	0.52	156.0	4.5	1.67	19.0	-24.0	0.06	37.0	0.68	-76.0
5000	0.53	140.0	2.6	1.35	-3.0	-23.0	0.08	35.0	0.71	-96.0
6000	0.48	120.0	0.9	1.11	-22.0	-21.0	0.09	34.0	0.73	-112.0

HEWLETT PACKARD

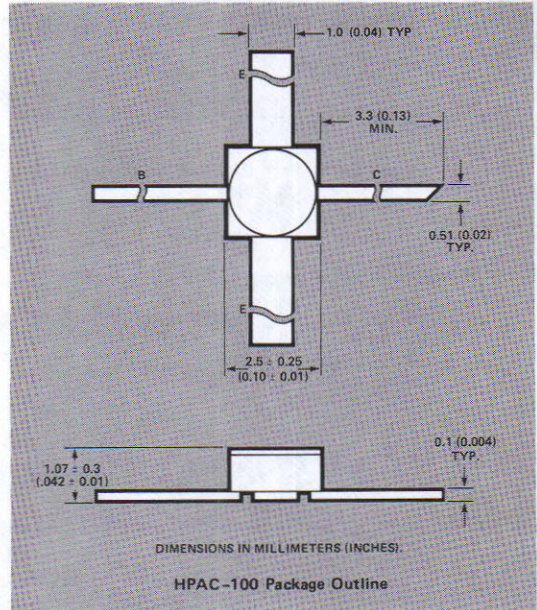
LOW NOISE TRANSISTOR

HXTR-6105

Bipolar Transistors

Features

LOW NOISE FIGURE
  4.2 dB Maximum at 4 GHz Guaranteed
HIGH GAIN
  9 dB Typ. at NF Bias Conditions
WIDE DYNAMIC RANGE
RUGGED HERMETIC PACKAGE
  Co-fired Metal/Ceramic Construction



HPAC-100 Package Outline

Description

The HXTR-6105 is an NPN bipolar transistor designed for low noise at 4 GHz with high output dynamic range. This transistor also features high output power and high gain at the NF bias and tuning conditions.

The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture,and the chip is provided with a dielectric scratch protection over its active area.

The HXTR-6105 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at $V_{CB} = 15V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$	3076.1*	–	50	120	220
F_{MIN}	Minimum Noise Figure f = 1.5 GHz = 4 GHz	3246.1	dB		2.2 3.8	 4.2
G_a	Associated Gain f = 1.5 GHz = 4 GHz		dB	 8.0	15.0 9.0	
P_{1dB}	Associated Power Output at 1dB Compression at 4 GHz $V_{CE} = 15V$, $I_C = 15mA$		dBm		14	
M_{MIN}**	Minimum Noise Measure $V_{CE} = 15V$, $I_C = 15mA$, f = 4 GHz		dB		4.2	4.7

*300 μs wide pulse measurement at ≤ 2% duty cycle.

**$M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5×10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 4.8 mW/° C, $T_C \geq$ 106° C.

Absolute Maximum Ratings *

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

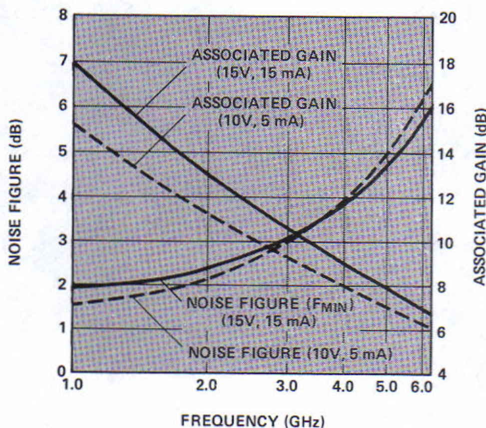


Figure 1. Typical F_{MIN} and Associated Gain vs. Frequency.

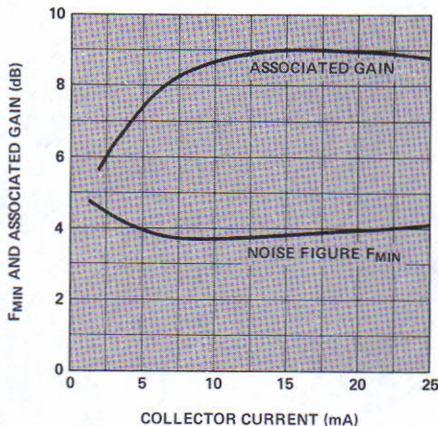


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 4 GHz for V_{CE}=15V (Tuned for F_{MIN}).

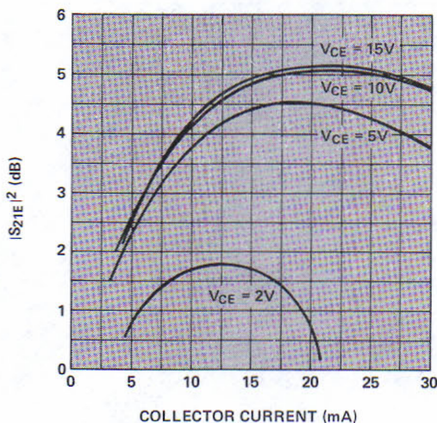


Figure 3. Typical $|S_{21E}|^2$ vs. Current at 4 GHz.

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.238/123°	6.81	1.80
1500	.385/142°	5.33	2.15
2000	.429/173°	5.04	2.25
3000	.541/-158°	6.54	3.01
4000	.628/-135°	15.54	3.81
5000	.624/-107°	60.14	4.75

Figure 4. Typical Noise Parameters at V_{CE}=15V, I_C=15mA.

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.66	-52	29.0	28.3	152	-39.2	0.01	69	0.90	-16
500	0.59	-139	22.0	12.5	101	-37.7	0.03	41	0.55	-33
1000	0.59	-169	16.5	6.71	80	-29.6	0.03	45	0.47	-37
1500	0.59	177	13.1	4.54	65	-27.5	0.04	49	0.47	-41
2000	0.61	165	10.8	3.48	53	-25.5	0.05	50	0.47	-50
2500	0.60	159	8.8	2.75	43	-24.0	0.06	51	0.49	-61
3000	0.62	148	7.2	2.28	32	-22.7	0.07	52	0.50	-68
3500	0.62	141	5.7	1.93	21	-21.4	0.09	49	0.54	-80
4000	0.62	132	4.6	1.70	10	-20.0	0.10	47	0.57	-85
4500	0.60	126	3.5	1.50	0.0	-19.0	0.11	45	0.60	-94
5000	0.60	118	2.6	1.35	-9	-17.2	0.14	42	0.65	-102
5500	0.61	112	1.8	1.23	-20	-16.8	0.14	35	0.66	-112
6000	0.62	104	0.9	1.11	-29	-16.1	0.16	31	0.67	-122

HEWLETT PACKARD

LOW NOISE TRANSISTOR

HXTR-6106

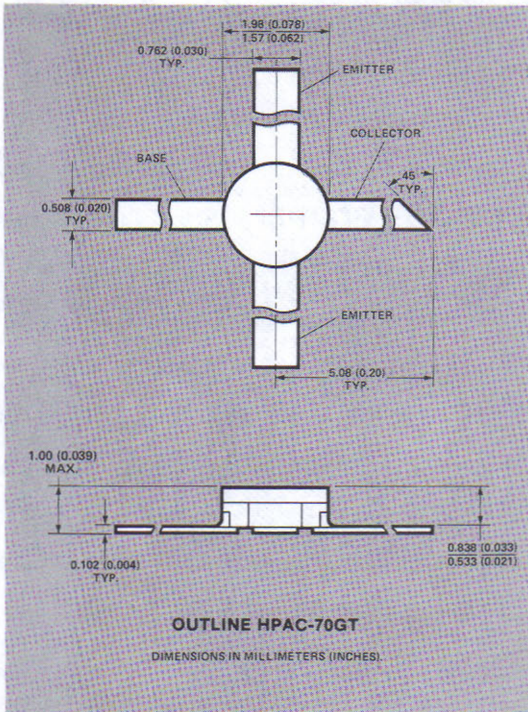
Features

GUARANTEED LOW NOISE FIGURE
2.7 dB at 2 GHz Max., 2.5 dB Typical
3.8 dB at 4 GHz Typical

HIGH ASSOCIATED GAIN
11.5 dB Typical at 2 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Description

The HXTR-6106 is an NPN bipolar transistor designed for low noise up to 6 GHz with wide dynamic range. This transistor also features high output power and high gain at the NF bias and tuning conditions.

The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture, and the chip is provided with a dielectric scratch protection over its active area.

The HXTR-6106 is supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$		3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$		3076.1*	—	50	120	220
F_{MIN}	Minimum Noise Figure	f=2 GHz	3246.1	dB		2.5	2.7
		4 GHz				3.8	
G_a	Associated Gain	f=2 GHz			10.0	11.5	
		4 GHz				9.0	
P_{1dB}	Associated Power Output at 1dB Compression $V_{CE} = 15V$, $I_C = 10mA$	f=2 GHz		dBm		15	
M_{MIN}	Minimum Noise Measure $V_{CE} = 15V$, $I_C = 10mA$, f = 2GHz			dB		2.6	3.0

*300μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to reduce median time to failure (MTTF) of 3.5×10^6 hours at T_J = 125° C (based on Activation Energy = 1.1 eV).
2. T_{CASE} = 25° C.
3. Derate at 5.4 mW/° C, $T_C \geq 117$° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

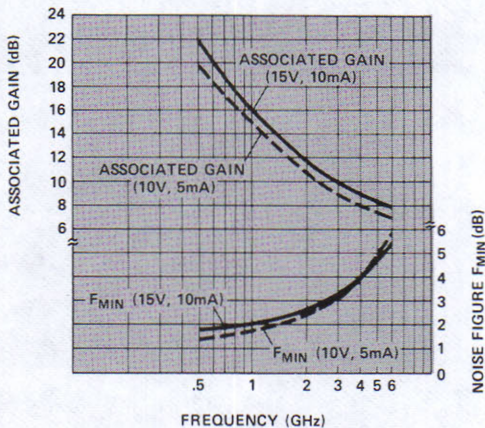


Figure 1. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency.

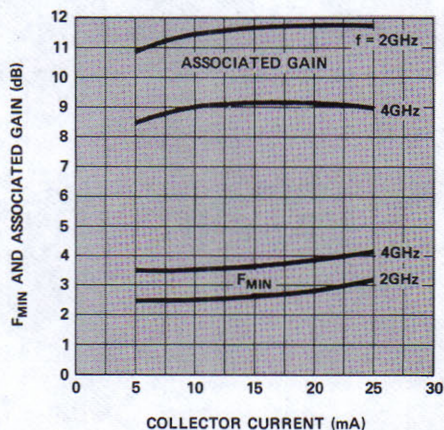


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Current at 2 GHz and 4 GHz at V_{CE} = 15V (Tuned for F_{MIN}).

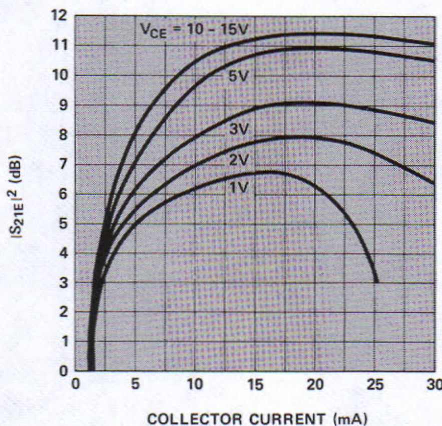


Figure 3. Typical $|S_{21E}|^2$ vs. Current at 2 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 10mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.77	-36	26.4	20.8	157	-38.4	0.012	67	0.93	-12
200	0.72	-70	25.6	19.0	139	-34.0	0.020	55	0.82	-21
300	0.70	-95	24.1	16.0	125	-32.0	0.025	46	0.71	-26
400	0.70	-113	22.7	13.6	115	-31.0	0.028	41	0.64	-29
500	0.69	-126	21.3	11.6	108	-30.5	0.030	37	0.59	-31
600	0.68	-136	20.1	10.1	102	-29.9	0.032	36	0.56	-33
700	0.67	-143	19.0	8.9	97	-29.6	0.033	35	0.54	-34
800	0.66	-149	18.0	7.9	93	-29.4	0.034	35	0.54	-35
900	0.66	-154	17.0	7.0	91	-29.1	0.035	34	0.53	-36
1000	0.66	-159	16.1	6.4	86	-28.9	0.036	35	0.53	-36
1500	0.68	-174	12.8	4.3	72	-27.0	0.040	36	0.48	-41
2000	0.66	177	10.5	3.3	61	-27.1	0.044	40	0.50	-51
2500	0.68	169	8.5	2.6	50	-26.2	0.049	42	0.50	-60
3000	0.67	163	7.0	2.2	39	-25.0	0.056	44	0.54	-67
3500	0.69	156	5.6	1.9	31	-24.1	0.062	46	0.54	-77
4000	0.68	152	4.5	1.7	21	-23.1	0.070	46	0.60	-85
4500	0.69	142	3.6	1.5	12	-22.2	0.078	47	0.60	-92
5000	0.71	138	2.5	1.3	4	-21.2	0.087	46	0.62	-102
5500	0.70	130	1.8	1.2	-5	-20.5	0.094	42	0.66	-111
6000	0.76	124	0.9	1.1	-13	-19.7	0.103	42	0.67	-120
6500	0.71	121	0.0	1.0	-23	-19.1	0.111	38	0.75	-129

Typical Noise Parameters

Freq. (GHz)	F_{min} (dB)	G_a (dB)	Γ_o	R_N (Ω)
1.0	1.8	14.3	.10/60	48.9
1.5	2.1	13.3	.27/132	19.1
2.0	2.4	11.6	.46/156	9.9
3.0	3.4	8.9	.53/167	8.4
4.0	4.3	6.9	.61/174	6.4

Figure 4. Typical Noise Parameters at V_{CE} = 10V, I_C = 5mA.

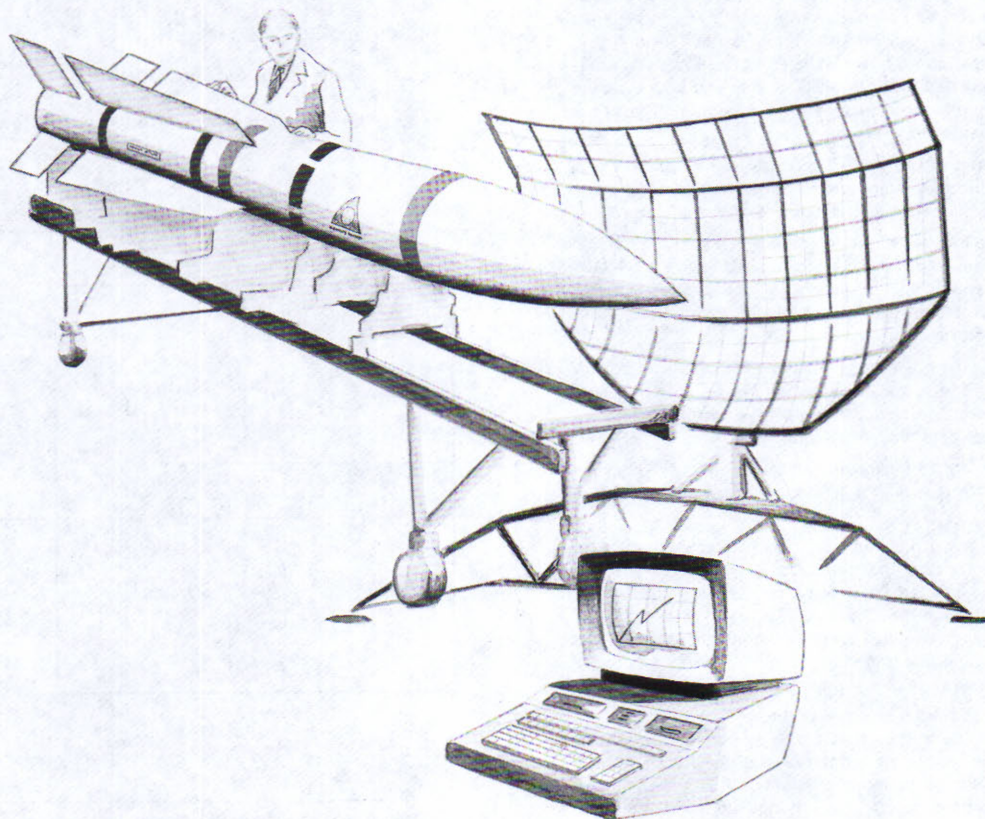
Applications for Bipolar Transistors

Bipolar Transistors

A 4.3 GHz Oscillator Using the HXTR-4101 Bipolar Transistor 72

A Cost-Effective Amplifier Design Approach at 425 MHz Using the HXTR-3101 Silicon Bipolar Transistor 73

The Design of a 900 MHz Oscillator with the HXTR-3102 76



HEWLETT PACKARD

APPLICATIONS FOR SILICON BIPOLAR TRANSISTORS

A 4.3 GHz Oscillator Using the HXTR-4101 Bipolar Transistor

(Portion of Application Note 975)

The basic condition for stable oscillation is a load impedance whose real and imaginary parts are equal in magnitude and opposite in sign to the impedance of the transistor. Computer programs are available to provide this load impedance when given the transistor S-parameters. Since these parameters are printed on the data sheet, the circuit is easily designed.

Since the condition for oscillation is satisfied, this circuit should oscillate. However, the S-parameters are measured at a small signal level and S-parameters change when power is increased. This change causes the negative resistance magnitude to decrease below the load resistance so that the condition for oscillation is no longer satisfied. The oscillation stops before it can be detected.

It appears that a two step process is necessary to design oscillators with small signal S-parameters. First the transistor is installed in a non-oscillating circuit. The impedance of this circuit is then measured with a network analyzer over a range of input power. The reflected power, which is greater than the input power, is noted. The added power (reflected minus input) will reach a maximum. The impedance at this power level is recorded.

The final step in the design process is the addition of a matching circuit to transform the load to the negative of the recorded impedance at maximum added power.

To illustrate this technique the details of a 4.3 GHz oscillator design will be given. This oscillator uses an HXTR-4101 transistor and forms the basis for the production test oscillator for this device. Collector-base voltage (V_{CB}) is 15 volts. Collector current (I_C) is 30 mA.

The HXTR-4101 is a common base NPN bipolar transistor characterized for oscillator applications. Each lot is tested in this circuit. The device is supplied in the HPAC-100, a rugged metal/ceramic hermetic package.

It is convenient to design for an impedance of -50 ohms looking into the oscillator. The topology chosen is shown in Figure 1.

The optimization program reduced the error function to zero by increasing the emitter stub length to 2.96mm (0.117 inch) and the base stubs to 7.86mm (0.031 inch). The transmission line is 0.79mm (0.031 inch) Duroid microstrip with effective dielectric constant of 1.9. This circuit was built and impedance measured on the network analyzer for a range of input power.

Since the resistance is negative the reflection coefficient exceeds unity and the impedance lies outside the normal Smith Chart. Although a compressed chart (outer circle corresponds to reflection coefficient of 3.16) may be used, it is more convenient to interchange test and reference arms on the network analyzer. This inverts the reflection coefficient so that the analyzer shows the circuit impedance with the sign changed. This is exactly the impedance that must be connected to the circuit to complete the oscillator.

Figure 2 shows the measured negative admittance of this circuit as a function of added power. This load line indicates the load for maximum added power is a normalized admittance of 0.26 + j0.32. This maximum added power, 19.6 dBm, is also the power output to be expected when the oscillator is completed.

Final Circuit

This circuit was built as described. Oscillation frequency was 4.0 GHz with power output 14 dBm. Slight adjustments of the open line lengths corrected the frequency to the desired 4.3 GHz and the power output to 20.5 dBm, close to the predicted 19.6 dBm.

Figure 3 shows the phase noise characteristics of the oscillator. At frequencies closer to the carrier the noise increases. This behavior is typical of many microwave oscillators.

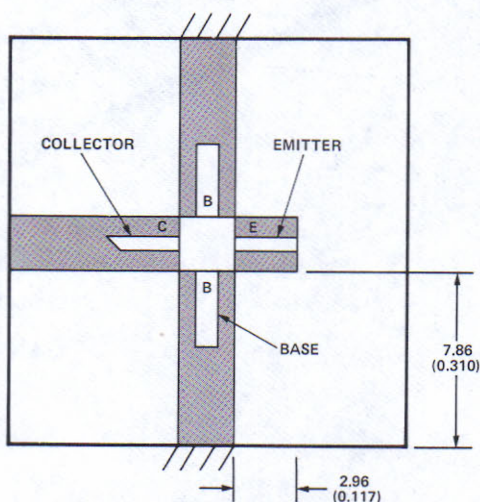


Figure 1. Topology of Non-Oscillating Circuit.

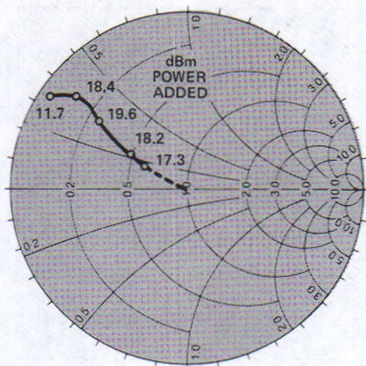


Figure 2. Admittance Load Line.

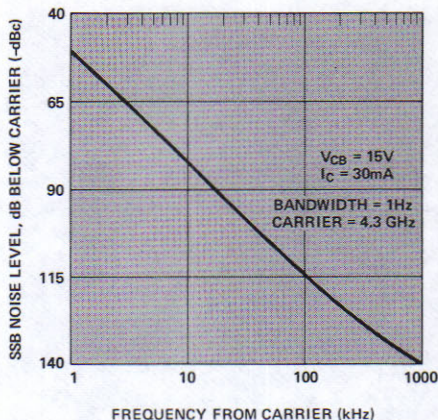


Figure 3. Phase Noise.

A Cost-Effective Amplifier Design Approach at 425 MHz Using the HXTR-3101 Silicon Bipolar Transistor

(Portion of Application Note 980)

INTRODUCTION

Cost vs. performance trade-offs at UHF frequencies are the primary considerations in any design of an amplifier gain stage. Balancing performance specifications and component cost is often difficult. One way to help solve this difficulty is by using low cost, off-the-shelf component parts and a cost-effective transistor.

This application note presents a straight forward design of a general purpose amplifier gain stage operating from 375 to 475 MHz, using the cost-effective HXTR-3101. This type of amplifier may be useful as the first or second stage of a multi-stage amplifier, where gain flatness, group delay variations, and input/output match are important.

AMPLIFIER DESIGN

Design Objectives

The design specifications for this amplifier stage design were chosen to be similar to many general amplifier gain stages at UHF frequencies.

Frequency Range 375 to 475 MHz
Gain $\geq$ 12 dB
Gain Flatness $\leq$ 0.5 dB
Input/Output SWR $\leq$ 1.5:1
Group Delay Variation $\leq$ .02ns/MHz
Bias Conditions V_{CE} = 10 V, I_C = 10 mA

In addition to the above design objectives, other objectives were to achieve cascadeability and simplicity of circuit design.

Characteristics of the HXTR-3101

Typically, for many higher gain UHF transistors, K is less than one, at frequencies less than 1 GHz. Such is the case for the HXTR-3101. One approach to a stable design under these conditions is to compensate the negative real impedance with a series loss element in the form of a resistor in series with the base of the transistor. As seen in the example below, this allows a particularly simple (low component count) matching circuit design to achieve low cost, broadband, well-matched gain performance. For lower-noise designs, conventional lossless matching can be used with proper allowance for the conditional stability (where K<1), with some trade-off in the other amplifier specifications.

Matching Network Designs

Input Matching Network — In selecting an appropriate value for the base resistor, Γ''_{MS} (the equivalent source impedance of the network consisting of the transistor and the base resistor) was monitored. It was found that Γ''_{MS} at 400 MHz, moved along a constant reactance line on the Smith Chart as the value of the resistor varied (See Figure 1). Further, it was found that a resistor value of 44 ohms, matched the input of the device close to 50 ohms. This matching condition eliminates the need for any extra matching elements (at least two), and greatly simplifies the input matching network which was of primary concern.

Output Matching Network — The output matching network, which consisted of a shunt L and series C, was designed using classical Smith Chart design techniques.

The complete R.F. amplifier design is shown schematically in Figure 2.

Attempts to reduce the gain flatness through computer optimization resulted in SWR degradation. Gain compensation techniques offer an approach which will improve the gain flatness as well as maintaining good SWR.

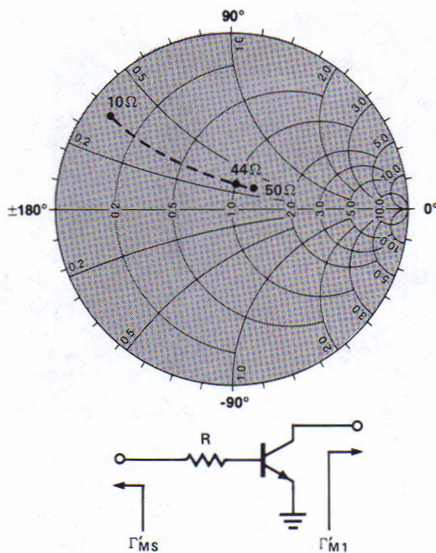


Figure 1. Γ'_{MS} **(equivalent source impedance for the network consisting of the transistor and the series base resistor) as a Function of Base Resistance.**

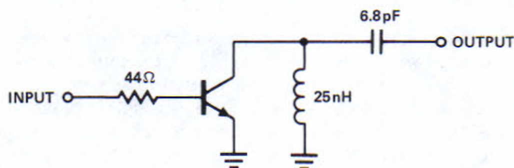


Figure 2. Completed R.F. Amplifier Design.

Gain Compensation

One type of dissipative compensation that can help improve the gain flatness and output match uses a diplexer. The simplest diplexer uses an L-C-R network shown in Figure 3.

By selecting the appropriate element values, the diplexer input will always present a 50 ohms input impedance when each output is terminated with 50 Ω.[1,2]

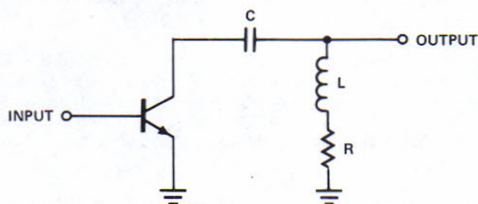


Figure 3. Diplexer Network: Simplified C, L, and R.

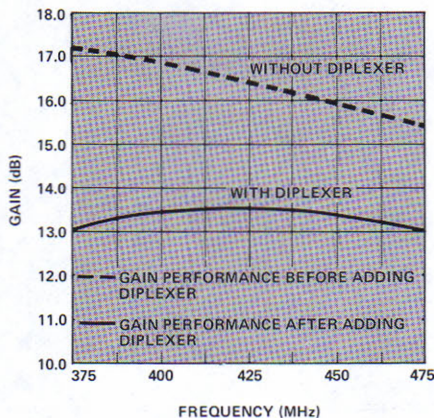


Figure 4. Amplifier Gain Performance vs. Frequency.

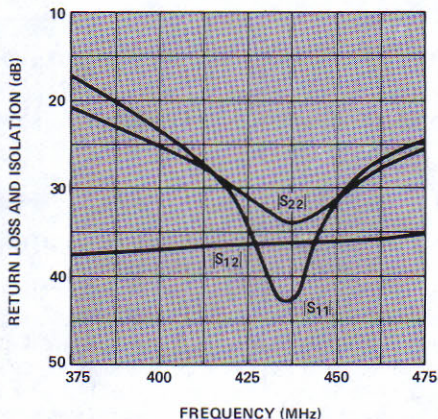
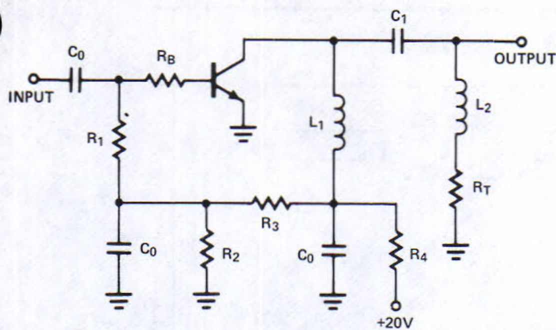


Figure 5. Amplifier Performance (with Diplexer added): Input Return Loss $|S_{11}|$**, Output Return Loss** $|S_{22}|$**, and Reverse Isolation** $|S_{12}|$ **vs. Frequency.**

PERFORMANCE

After the amplifier design was completed, standard resistor and capacitor values, which were close to the design values, were used in constructing the amplifier. The final amplifier performance is displayed in Figures 4 and 5. Figure 4 displays the gain performance before and after the addition of the diplexer. The final amplifier gain peak is 13.3 dB, and the gain flatness is within 0.5 dB. Figure 5 displays the final amplifier matching characteristics and the reverse isolation of the amplifier. The input and output SWR are better than 1.5:1 across the band of interest. The group delay variation is less than 0.01ns/MHz. Although the output power was not of primary concern, it was measured at 425 MHz and is +12 dBm (P_{1dB}).



COMPONENTS PARTS LIST

RESISTORS – R-oHm Corp. R-25 Carbon Film

R_B	46.7Ω	1/4 W
R_T	51.2Ω	1/4 W
R_1	6.8KΩ	1/4 W
R_2	1KΩ	1/4 W
R_3	6.8KΩ	1/4 W
R_4	900Ω	1/4 W

CAPACITORS – Erie Tech. Products Inc., "Red Cap" Ceramic Capacitors

C_0	1000pF	8101-100-Z5U-102K
C_1	3.3pF	8101-100-COGO-330C

INDUCTORS – All inductors were hand wound using 0.330mm (0.013 inch) diameter wire.

L_1	23 nH	Coil Dimensions 2.388mm (0.094 inch) Diameter 7.620mm (0.300 inch) Length/4 turns.
L_2	17 nH	Coil Dimensions 2.388mm (0.094 inch) Diameter 5.080mm (0.200 inch) Length/3 turns.

Figure 6. Complete Amplifier Circuit (D.C. and R.F.) Including Parts List.

CONSTRUCTION DETAILS

Both the R.F. and D.C. portions of the amplifier with components parts list is shown in Figure 6. All resistor and capacitor values used were standard values. Standard element values were used because of their easy accessibility. The inductors were hand wound using 0.330 mm (0.013 inch) diameter silver plated wire.

The D.C. bias network chosen uses voltage feedback and a constant base current source. The passive bias network is effective in minimizing changes to the quiescent point due to variations in temperature. By adjusting R_1 and R_2 this bias network can accommodate any value of h_{FE}.

The amplifier was built on "FR-4", 0.787 mm (0.031 inch) thick, 1/2 oz. copper clad (both sides), epoxy/fiberglass board. The relative dielectric constant, ϵ_r, is 4.95. The final board layout is shown in Figures 7a (top) and 7b (bottom), with component placement. Rivets were placed through the board on the emitter soldering pads to reduce the parasitic emitter inductance. The rivet diameter was 0.508 mm (0.020 inch). Even though rivets were used in this design, a practical, suitable alternate approach is plated-through holes.

The amplifier was housed in a Modpak™ Box, kit number 7022-4. The dimensions of the box are 31.750 mm (1.250 inch) x 63.500 (2.500) x 25.400 (1.000). The SMA connectors and the D.C. bias feed throughs were included in the kit.

CONCLUSIONS

This application note has presented the HXTR-3101 in a typical general purpose amplifier gain stage design. The amplifier design presented was cost effective in that it used very simple matching networks and off-the-shelf standard component values. Also, various design trade-offs were presented and discussed.

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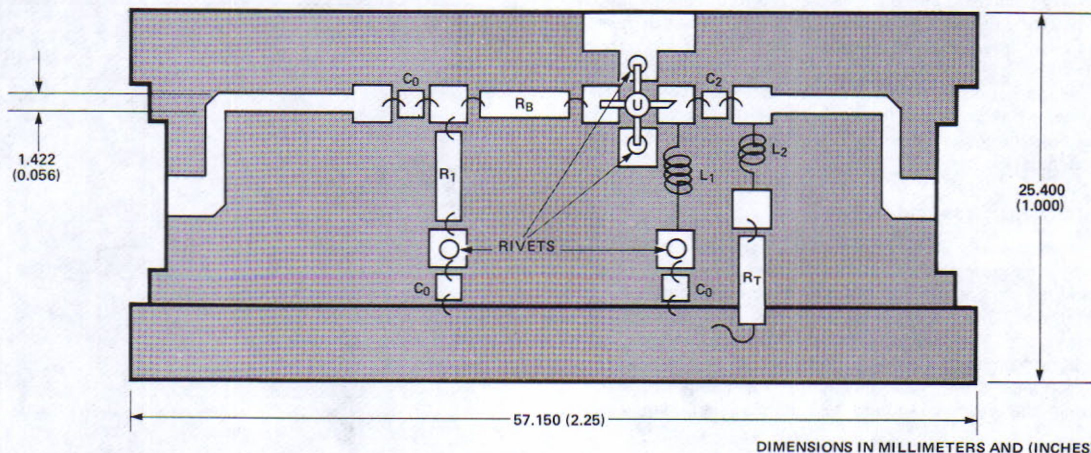


Figure 7a. Circuit Board Layout and Component Placement (Top View).

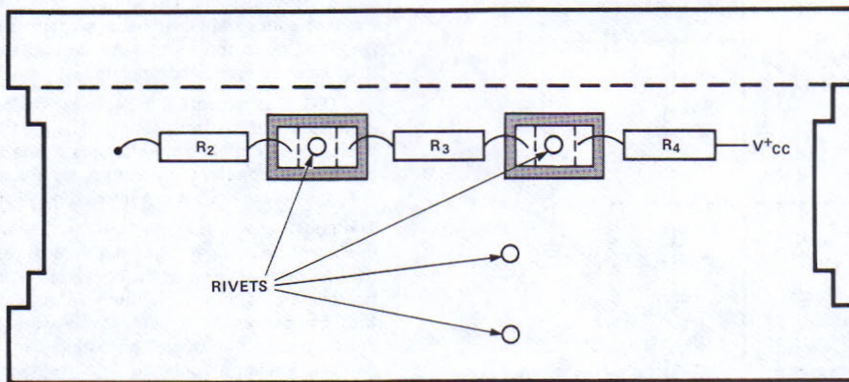


Figure 7b. Circuit Board Layout and Component Placement (Bottom View).

The Design of a 900 MHz Oscillator With The HXTR-3102

(Portion of Application Note 981)

INTRODUCTION

Designing a microwave transistor oscillator can be greatly simplified by using a procedure that utilizes both the device line[1,2] and load-pull[3] measurement techniques. The device line technique requires an initial circuit that has a negative input resistance at the design frequency but does not oscillate when loaded by the 50Ω test system. The optimum load impedance required for maximum power output can then be obtained by measuring the device line. However, if the load impedance is equal to the input impedance but differs in sign, then an initial transient oscillation will occur. This oscillation will change the transistor's S-parameters; consequently, the input impedance of the initial circuit changes, and the circuit may or may not produce steady-state oscillation. If the circuit oscillates, then the device line technique cannot be applied. With the load-pull technique, an initial circuit that is already oscillating can be characterized to obtain the load impedance needed for optimum power output at or near the initial frequency of oscillation. Thus, depending upon whether the initially designed circuit produces steady state oscillation or not, the design can be completed with either the load-pull or device line techniques. The test systems for both methods and their utilization are described in Appendix 1.

DESIGNING THE OSCILLATOR

The small signal S-parameters of the transistor, biased as shown in Figure 1, were first measured. An initial topology was then generated for this S-parameter representation of the device. This initial topology consisted of a shorted 50Ω stub and a 75Ω open stub connected, respectively, to the base and emitter as shown in Figure 2. The line lengths (ℓ_1, ℓ_2) were then computer optimized with Compact[4] to obtain dimensions required for an input impedance of -50Ω.

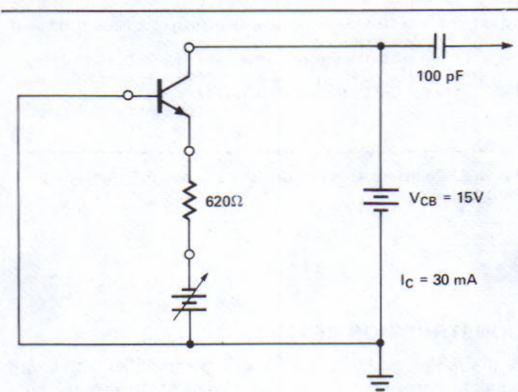


Figure 1. D.C. Bias Circuit.

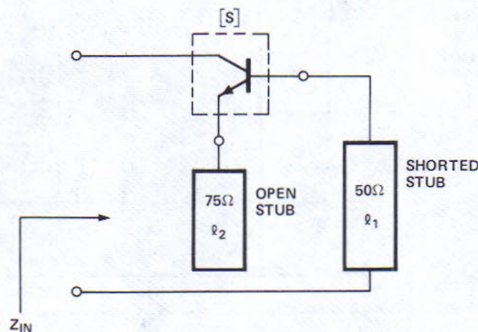


Figure 2. Initial Topology.

This circuit, built on Duroid[5] 5880 circuit board (0.31 inch thickness) oscillated at several frequencies. Signals in the vicinity of the design frequency were observed to be at higher power levels than frequencies further away. However, neither design method could be successfully applied because of these multiple oscillations.

Another initial circuit with a lower negative impedance (-40Ω) was then designed, and this circuit oscillated at 880 MHz with an output power of 15 dBm. The lower negative resistance value (-40Ω) may have changed the steady state negative input resistance at frequencies other than 880 MHz to values significantly below the 50Ω load impedance, and thus the circuit no longer oscillated at those frequencies.

Since this circuit was already oscillating, the load-pull method was applied to obtain the impedance required for maximum power output. A power output of 22.8 dBm was obtained at a frequency of 890 MHz. A simple matching network, consisting of a single 50Ω open stub was then designed. Slight adjustments of this stub and the open emitter stub were required to complete the design. The final circuit layout and a comparison of the final versus computed dimensions are shown in Figure 3.

OSCILLATOR PERFORMANCE

The final oscillator circuit produced an output power of 23.2 dBm at 900 MHz using a dc bias of V_{CB} = 15 volts and I_C = 30 mA. A very high efficiency (44%) was obtained. Figure 4 shows the effect of dc bias on power output. It was observed that slightly better efficiency (about 46%) was obtained at about 20 mA collector current for all voltages used.

Figure 5 shows the oscillator's phase noise performance as well as that for a similar microstrip 4.3 GHz bipolar transistor oscillator[6] using the HXTR-4101 — a device with geometry similar to the HXTR-3102. The HXTR-3102 oscillator's phase noise is approximately 5 dB lower. Although the difference in frequency does not make this a direct comparison, it is assumed that the performance difference is related to the difference in circuit Q.

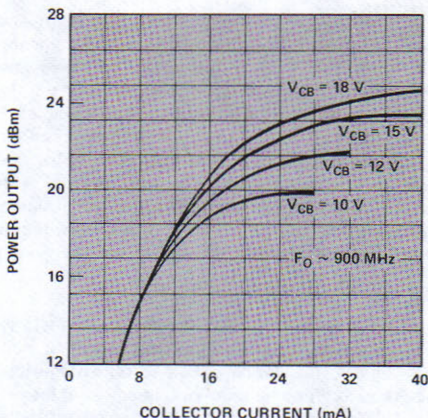


Figure 4. Power Output vs. Bias.

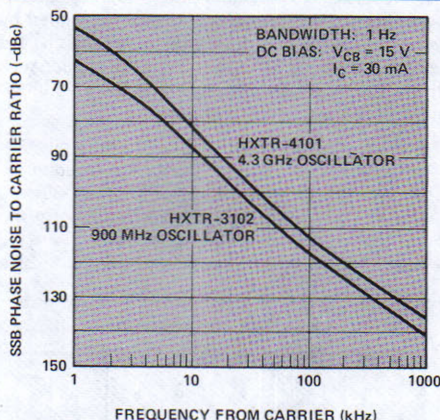
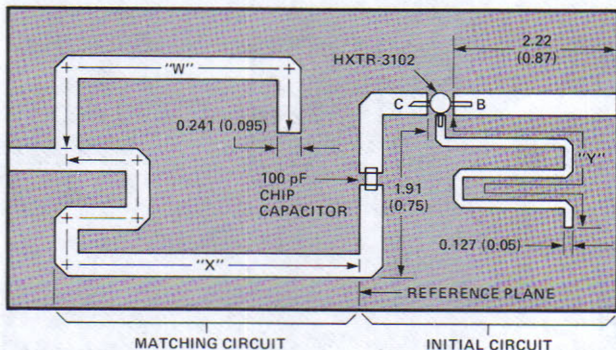


Figure 5. Phase Noise.



DIMENSIONS	LENGTHS			
	COMPUTED		FINAL	
	(cm)	(in.)	(cm)	(in.)
"W"	4.97	1.96	5.08	2.00
"X"	7.73	3.04	7.73	3.04
"Y"	6.19	2.43	6.35	2.50

CIRCUIT BOARD MATERIAL: DUROID 5880 (0.031 INCH THICKNESS)
DIMENSIONS IN CENTIMETERS (INCHES).

Figure 3. Final Oscillator Circuit Layout.

CONCLUSION

A combination of the load-pull and device line measurement techniques can simplify the design of microwave transistor oscillators. Depending upon whether or not the initial circuit, designed with the small signal S-parameters of the transistor, produces steady-state oscillation, one of these methods can be selected and used to obtain the optimum load required for maximum output power. This was shown to be a useful design procedure in the design of a very efficient 900 MHz microstrip oscillator with the HXTR-3102 bipolar transistor.

APPENDIX I

Figure 6 shows a block diagram of the device line test system. This system can be used to characterize a non-oscillating negative resistance circuit to obtain the load impedance required for maximum output power at the test frequency. This information is obtained by reversing[1,7] the harmonic converter (Hewlett-Packard model 8411A) so that the displayed impedance is the actual load impedance needed. By recording the incident power as a function of the power reflected from the circuit, the power added by the negative resistance network can be computed as the difference between these two power levels. The impedance at which the added power is maximum is the load impedance that must be presented to the circuit.

Figure 7 shows the block diagram for the load pull test system. This system can be used to obtain the load impedance required to complete the design of an already oscillating network. As with the device line test system, the harmonic converter is again reversed. However, since the oscillating device itself is the signal source during the test, a reference plane calibration must initially be made by connecting a sweep oscillator and a short in place of the tuner and oscillating circuit respectively. The sweep oscillator should be set to sweep about the frequency of the test circuit. The line stretcher is then adjusted to obtain a cluster on the left side (at $\Gamma = 1 \angle \pm 180°$) of the polar display. The sweep oscillator and short are then removed, and the oscillating network and tuner are reinstalled in the system. The tuner can then be adjusted for maximum power at or near the frequency of interest. If the spectrum observed on the spectrum analyzer shows a stable single frequency oscillation, the impedance displayed will be the load impedance needed to design the output network.

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4. Compact Engineering, a Division of CGIS, 1131 San Antonio Road, Palo Alto, CA 94303.
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6. Paul Ramratan et al, *"FET vs. Bipolar: Which Oscillator is Quieter?"* Microwaves, Volume 19, pp. 82-83 (November 1980).
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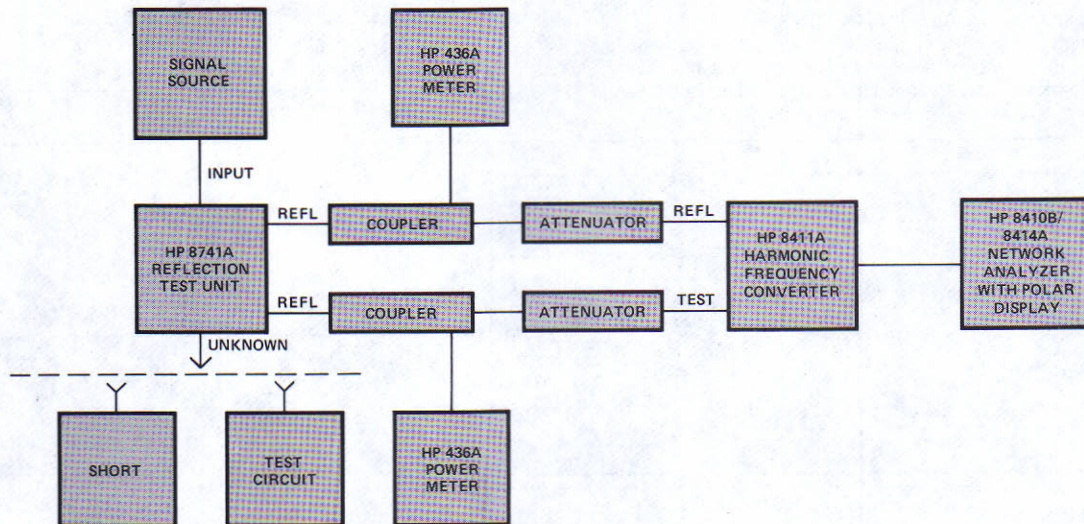

Figure 6. The Device Line Test System.

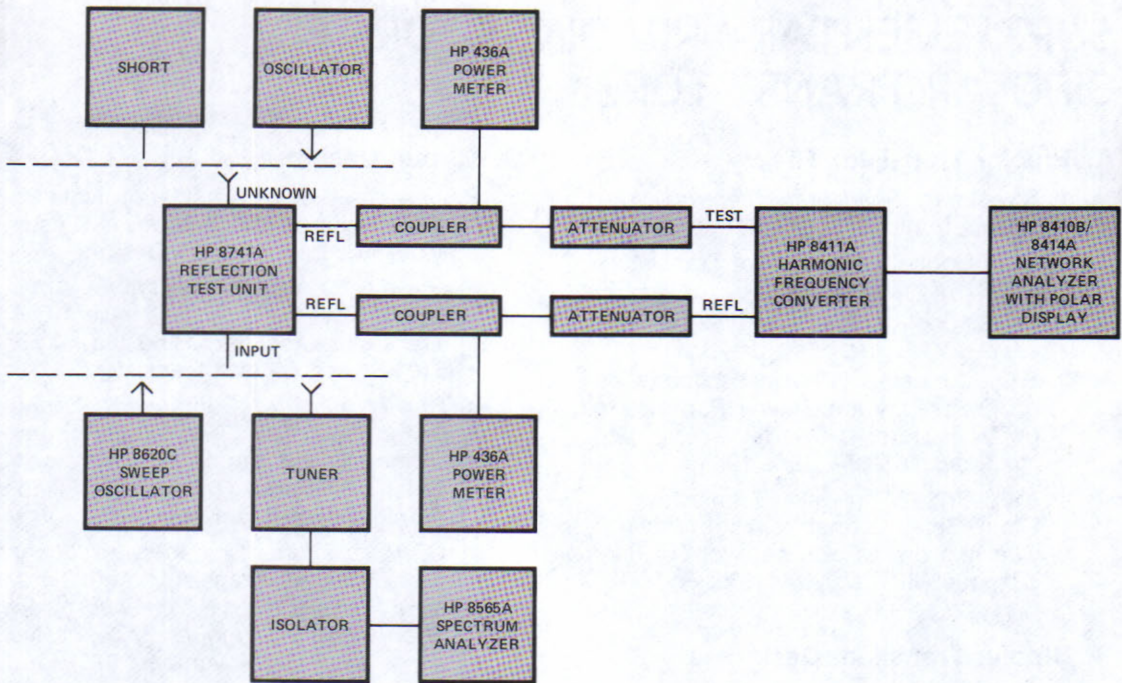

Figure 7. Load-Pull Test System.

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*2. H.F. Cooke, "Microwave Transistors — Theory and Design," *Proc. IEEE,* vol. 59, No. 8, pp. 1163-1181, August 1971.

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B. Bipolar Transistor Design

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8. *Hewlett-Packard* Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design."

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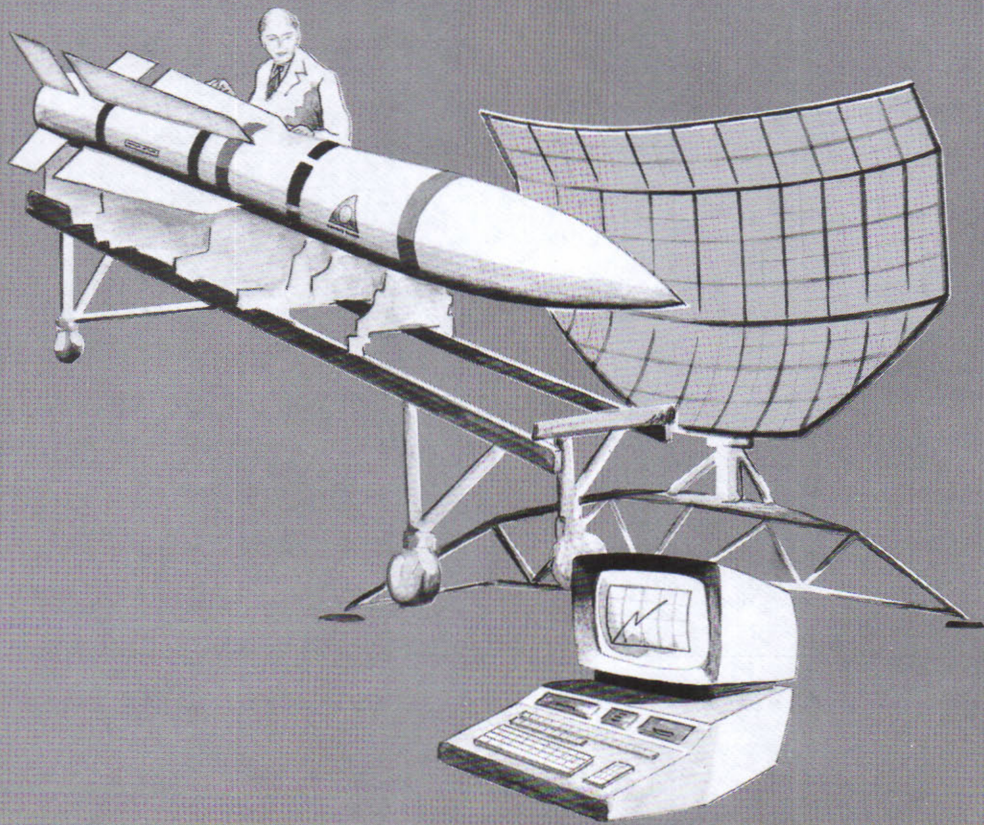
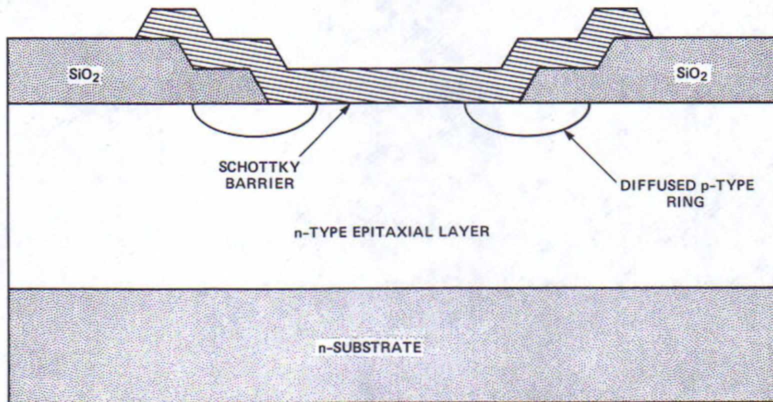


Schottky Barrier Diodes

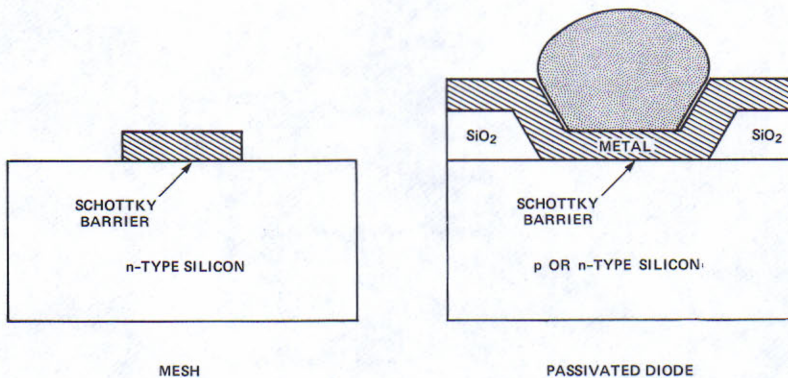
A Schottky barrier diode contains a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The resulting non-linear diode is similar to point contact diodes and p-n junction diodes. The Schottky diode is more rugged than the point contact diode because the contact is not subject to change under vibration. The advantage over the p-n junction is the absence of minority carriers which limit the response speed in switching applications and the high frequency performance in mixing and detecting applications.

Types of Diode Construction

There are several assembly geometries used for Schottky barrier diodes. Three types used in this catalog are shown in Figure 1.



HYBRID SCHOTTKY BARRIER DIODE



MESH

PASSIVATED DIODE

Figure 1. Three Types of Schottky Barrier Diodes

Mesh Diodes

The mesh diode is made by depositing metal through a screen to the semiconductor surface. Many closely spaced diodes are created on the chip. The diode contacts are too small for thermocompression bonding. Contact is made by pressing a sharp metal point against one of the metal contacts on the diode. The large number of contacts provide a good yield to this operation.

Although the mesh contacts are too small for thermocompression bonding, they are not small enough for operation at high microwave frequencies. It is not possible to deposit reliable contact areas small enough for operation at frequencies above 7 GHz; in fact, the highest test frequency is 3 GHz. These mesh devices have model numbers in the series 5082-2300, 2400, 2500 and 2900.

Passivated Diodes

The problem of creating small area contacts was solved by the development of the passivated diode process. An oxide layer is formed over the entire silicon area. Then photographic techniques are used to open a small hole in the oxide.

The appropriate metal is deposited in the hole to make the small area Schottky barrier. Then gold or silver is deposited to provide a surface for the thermocompression bond. This final metal area will overlap the oxide surface to provide a sufficiently large area. Passivated diodes include the 5082-2835, the 5082-2750 series, zero bias detectors, and all diodes in outlines 44 and 49. These devices are used at frequencies up to 40 GHz, although the highest test frequency is 16 GHz. The small area problem is solved, but the passivation process has a severe limitation on breakdown voltage. Reverse voltage at 10 microamperes current is less than ten volts. The highest guaranteed voltage in the catalog is three volts.

Hybrid Diodes

The breakdown voltage limitation was solved with the invention of the hybrid process. By combining a Schottky diode with a p-n junction the premature breakdown of the passivated diode is eliminated without sacrificing the picosecond switching response of the Schottky barrier. Breakdown voltage specifications as high as 70 volts are available. Hybrid diodes are numbered from 5082-2800 to 2826 and also 5082-2836.

The dual nature of the hybrid diode limits the lowest capacitance to a picofarad. This limits the high frequency guaranteed performance of these diodes to 2 GHz.

These hybrid chips are assembled in an inexpensive glass package (outline 15) with a C-shaped spring contact. The presence of the spring limits the speed of assembly and therefore the cost. The double stud package (outline 12) eliminates the spring by contacting the chip directly between two leads. A new hybrid chip was developed to withstand the higher temperatures used in this automatic assembly process. These low cost diodes are called HSCH-1001 or 1N6263.

The Height of the Schottky Barrier

The current-voltage characteristic of Schottky barrier diodes at room temperature is described by the following equation:

$$I = I_S \left(\exp\left(\frac{V - IR_S}{0.026} \right) - 1 \right)$$

For currents below 0.1 mA, the IR_S term may be neglected. On semi-log graph paper, as plotted in this catalog, the current graph will be a straight line with inverse slope 2.3 x 0.026 = 0.060 volts per cycle. All curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the type of metal deposited on the silicon and to the treatment of the silicon surface layer. The term "barrier height" is related to the voltage required for a given current. Low voltage corresponds to low barrier.

Study of the forward characteristics in this catalog shows that the lowest barrier diode is the HSCH-3486 family of zero bias detectors. Detection at zero bias is possible for a range of barrier heights, but the voltage sensitivity is best for high barrier diodes. The sensitivity degrades for barrier heights less than that of the HSCH-3486. The other extreme is represented by medium barrier mixer diodes such as the 5082-2701. However, this barrier height corresponds to a zero bias junction resistance that requires a load resistance above 10 megohms. Zero bias detection with these diodes is limited to single frequency applications.

Applications of Schottky Barrier Diodes

Schottky barrier diodes are useful in a wide variety of applications over a broad frequency range from digital to microwave.

General Purpose Diodes

The HSCH-1001 and similar diodes are useful for clipping, clamping, and speed up of transistor switching. These applications are discussed in Application Note 942, Schottky Diodes for High Volume Low-Cost Applications, and in several application bulletins described in the abstracts section of this catalog.

Mixers

The most sensitive receivers using Schottky barrier diodes make use of the nonlinear properties of the diode to produce a difference frequency by mixing the received signal with a local oscillator. Although this can be done with a single diode, it is more common to use multiple diodes in balanced or double balanced mixers. Balanced circuits reduce the effect of a noisy local oscillator and also reduce the level of high order mixing products that are not related to the desired input frequency. For multiple diode mixers, batch matched devices or matched pairs are available.

The most important property of mixer diodes is the noise figure — a measure of how small a signal can be received. The noise level for a perfect receiver is -114 dBm per MHz of bandwidth. A 6 dB noise figure mixer will degrade the noise level to -108 dBm per MHz. If the bandwidth of the receiver is 4 MHz the noise level is raised to -102 dBm. If a 10 dB signal to noise level is required for proper operation of the receiver, the sensitivity is -92 dBm. In this section of the catalog there are two groups of single diodes characterized for mixer applications. For stripline circuits the hermetic H-2, broadband C-2, and the less expensive E-2 outlines are available. The best diodes are guaranteed to have a noise figure less than 6.0 dB.

The other group of mixer diodes uses outline 15, glass package, for 2 and 3 GHz and outlines 44 and 49, ceramic packages, for 9.375 and 16 GHz. The best units have a 6 dB noise figure with the exception of the 16 GHz devices with a 6.5 dB prime unit.

Applications such as Doppler radar involving intermediate frequencies below 1 MHz will benefit by using the 5082-2400 or -2565 with its lower noise at these output frequencies. The additional noise (flicker noise) varies inversely with difference frequency and may differ as much as 20 dB from one diode type to another. Since the lowest capacitance (passivated) diodes (measured at 9.375 or 16 GHz) have the highest flicker noise, it is sometimes better to choose a Doppler mixer diode for lowest flicker noise rather than for lowest published noise figure.

There is one more type of mixer diode in this catalog — the quads for double balanced mixers in outlines E1, C4 and H4. These units contain a monolithic beam lead quad — four diodes connected in a ring configuration by gold deposited and plated on the wafer. Since the four diodes are made at the same time on the same portion of a wafer, they are nearly identical and ideally suited for double balanced mixers.

In most cases both medium and low barrier models are available. The low barrier units have an impedance closer to 50 ohms. These models give better performance in broad band untuned circuits, particularly in those applications with local oscillator power below normal.

Detector Applications

For system applications with relaxed requirements on sensitivity the video detector receiver is a good alternative to the superheterodyne receiver. The sensitivity is degraded about 50 dB, but the circuitry is simplified and broad bandwidth is easily attained without the problem of tracking the local oscillator frequency.

The important parameters are tangential signal sensitivity (TSS) and voltage sensitivity (γ). Both of these, as well as video resistance (Rv), are guaranteed for these detector diodes. Typical detector performance is shown for mixer diodes, but detector diodes are designed for superior performance for this application.

Tangential signal sensitivity measures the ability of the diode to distinguish a small signal from noise. The name relates to a type of radar display with the bottom of the signal pulse tangent to the top of the noise level. There are subjective aspects to this measurement so that TSS measurement is now made with a voltmeter. The value depends on diode noise as well as detection capability.

In some applications, the detector is used as a

monitor and the measurement level is well above the noise. For these applications, voltage sensitivity, voltage output for one microwatt input, is the important parameter.

The third specification, video resistance (R_V), is important for video amplifier and response time considerations. The video amplifier resistance, R_L, should be large compared to R_V because the maximum output voltage is degraded by the factor

$$\frac{R_L}{R_L + R_V}$$

However, response time is proportional to the RC product. If fidelity to pulse shape is important, the presence of pulses with steep edges requires a smaller value of load resistance. Sensitivity must be sacrificed for fidelity.

Zero bias Schottky detector diodes are available in the glass package (outline 15) and ceramic packages (outlines 44 and 49). Two types of metal to semiconductor junctions are used, resulting in two distinct ranges of junction resistance (video resistance). Since voltage sensitivity varies with resistance, the high resistance diodes have better voltage sensitivity. However, high resistance means higher noise so the TSS specifications are better for the low resistance diodes. All tests are done at 10 GHz.

The other type of detector diode (5082-2824 and -2750 series) requires a small forward bias. Production tests are made with 20 microamperes of bias which reduces the video resistance to about 1300 ohms. At zero bias the resistance is higher than for either one of the zero bias detectors. Although the statement has been made that high resistance corresponds to good sensitivity, the resistance is so high for these models (40 megohms for the 2750 series) that the sensitivity is degraded by normal load resistances. These diodes can be used without bias if the load resistance is comparable to the diode resistance. This is discussed in AN988 — All Schottky Diodes are Zero Bias Detectors.

The 5082-2824 diode is tested at 2 GHz. The 2750 series is supplied in outlines 15, 44, and 49 and tested at 10 GHz. The 5082-2787 is similar to the 2755 in outline 15 with the parameters sample tested to reduce cost.

Schottky Diodes Selection Guide

Detailed specifications are given on the pages listed. The primary applications are shown in this guide. Other applications are discussed in the text.

<table>
<tr><th rowspan="2">Package Outline</th><th colspan="4">Application</th></tr>
<tr><th>Mixer (Page Number)</th><th>Detector (Page Number)</th><th>Zero Bias Detector (Page Number)</th><th>General Purpose (Page Number)</th></tr>
<tr><td>E2, H2*, C2</td><td>91</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>E1, H4*, C4</td><td>99</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>44*, 49*</td><td rowspan="2">101</td><td rowspan="2">113</td><td rowspan="2">109</td><td>—</td></tr>
<tr><td>15*</td><td>86</td></tr>
<tr><td>12*</td><td>—</td><td>—</td><td>—</td><td>86</td></tr>
</table>

*Hermetic

HEWLETT PACKARD

SCHOTTKY BARRIER DIODES FOR GENERAL PURPOSE APPLICATIONS

1N5711*
1N5712*
5082-2301 (1N5165)
5082-2302 (1N5166)
5082-2303 (1N5167)
5082-2305
5082-2800/10/11/35*
5082-2900*
HSCH-1001 (1N6263)*

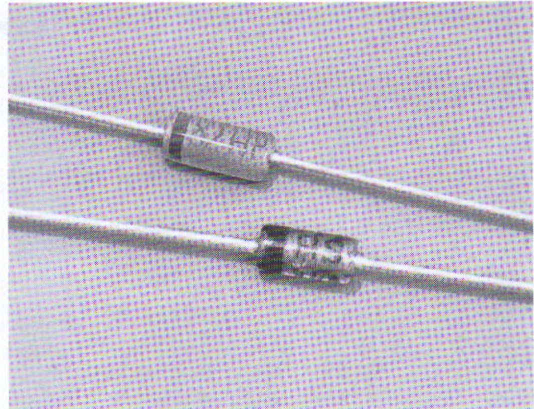
Features

LOW TURN-ON VOLTAGE: AS LOW AS 0.34V AT 1mA

PICO-SECOND SWITCHING SPEED

HIGH BREAKDOWN VOLTAGE: UP TO 70V

MATCHED CHARACTERISTICS AVAILABLE



Description/Applications

The 1N5711, 1N5712, 5082-2800/10/11 are passivated Schottky barrier diodes which use a patented "guard ring" design to achieve a high breakdown voltage. They are packaged in a low cost glass package. They are well suited for high level detecting, mixing, switching, gating, log or A-D converting, video detecting, frequency discriminating, sampling and wave shaping.

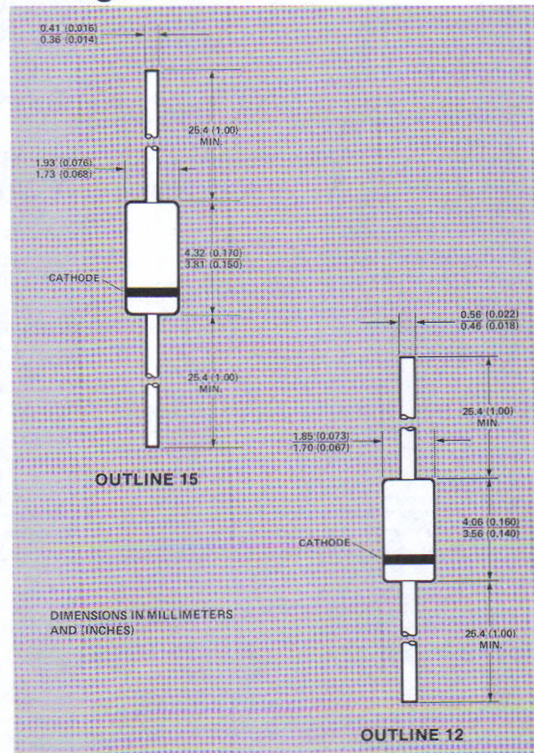
The 5082-2835 is a passivated Schottky diode in a low cost glass package. It is optimized for low turn-on voltage. The 5082-2835 is particularly well suited for UHF mixing.

The 5082-2300 and 2900 Series devices are unpassivated Schottky diodes in a glass package. These diodes have extremely low 1/f noise and are ideal for low noise mixing, and high sensitivity detecting. They are particularly well suited for use in Doppler or narrow band video receivers.

The HSCH-1001 is a Hybrid Schottky diode sealed in a rugged double stud Outline 12 glass package suitable for automatic insertion. The low turn-on voltage, fast switching speed, and low cost of these diodes make them ideal for general purpose switching.

Application Bulletins 13, 14, 15, and 16 describe applications in which these diodes are used for speed up of a transistor, clipping, clamping, and sampling, respectively. Other digital and RF applications are described in Application Bulletins 26, 27, 28, 30, 31 and 36.

Package Dimensions



*Also available in Tape and Reel. Please contact local HP Sales Office for further information.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range
5082-2305, 2301, 2302, 2303, 2900 -60°C to +125°C
1N5711, 1N5712, 5082-2800/10/11,
HSCH-1001 .... -65°C to +200°C
5082-2835 .... -60°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

DC Power Dissipation (Measured in an infinite heat sink)
Derate linearly to zero at maximum rated temperature
5082-2305, 2301, 2302, 2303, 2900 .... 125 mW
1N5711, 1N5712, 5082-2800/10/11 .... 250 mW
5082-2835 .... 150 mW
HSCH-1001 .... 400 mW

Peak Inverse Voltage .... V_{BR}

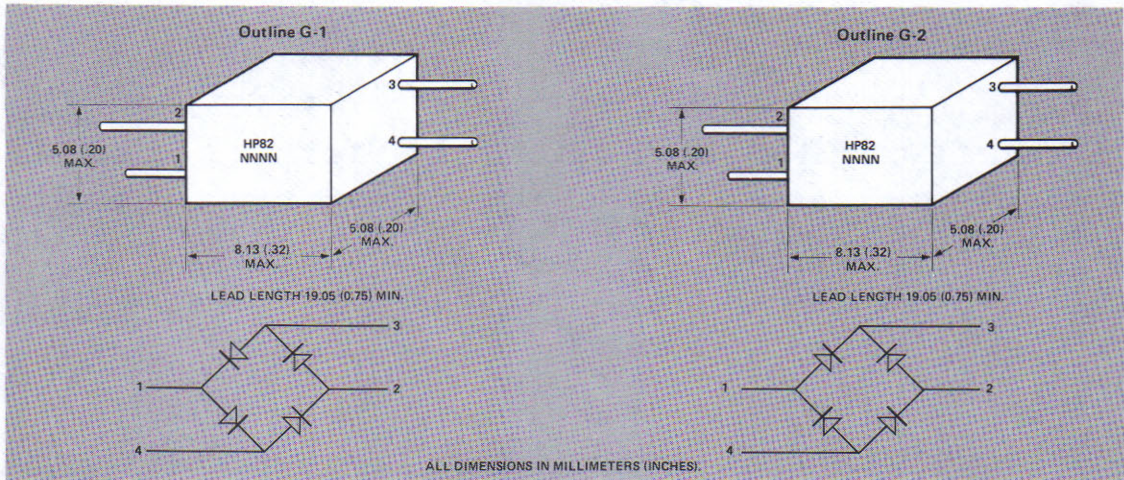
Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	V_F=1V Max at Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA)	at V_R (V)	Maximum Capacitance C_T (pF)
2800	15	70	410	15	200	50	2.0
1N5711	15	70	410	15	200	50	2.0
2305	15	30	400	75	300	15	1.0
2301 (1N5165)	15	30	400	50	300	15	1.0
2302 (1N5166)	15	30	400	35	300	15	1.0
2303 (1N5167)	15	20	400	35	500	15	1.0
2810	15	20	410	35	100	15	1.2
1N5712	15	20	550	35	150	16	1.2
2811	15	15	410	20	100	8	1.2
2900	15	10	400	20	100	5	1.2
2835	15	8*	340	10†	100	1	1.0
HSCH-1001 (1N6263)	12	60	410	15	200	50	2.2
Test Conditions		I_R = 10 µA *I_R = 100 µA	I_F = 1 mA	†V_F = .45V			V_R = 0 V f = 1.0 MHz

Note:
Effective Minority Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 20 mA except for HSCH-1001 (1N6263), 1N5711, and 1N5712 which are measured at 5 mA.

Matched Pairs and Quads

Basic Part Number 5082-	Matched Pair Unconnected	Matched Quad Unconnected	Matched Ring Quad Encapsulated G-1 Outline	Matched Bridge Quad Encapsulated G-2 Outline	Batch Matched	Test Conditions
2301	5082-2306 ΔV_F = 20 mV ΔCo = 0.2 pF					ΔV_F at I_F = 0.75, 20 mA ΔCo at f = 1.0 MHz
2303	5082-2308 ΔV_F = 20 mV ΔCo = 0.2 pF	5082-2370 ΔV_F = 20 mV ΔCo = 0.2 pF	5082-2396 ΔV_F = 20 mV ΔCo = 0.2 pF	5082-2356 ΔV_F = 20 mV ΔCo = 0.2 pF		ΔV_F at I_F = 0.75, 20 mA ΔCo at f = 1.0 MHz
2900	5082-2912 ΔV_F = 30 mV	5082-2970 ΔV_F = 30 mV		5082-2997 ΔV_F = 30 mV		ΔV_F at I_F = 1.0, 10 mA
2800	5082-2804 ΔV_F = 20 mV	5082-2805 ΔV_F = 20 mV			5082-2836* ΔV_F = 20 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 0.5, 5 mA *I_F = 10 mA ΔC_O at f = 1.0 MHz
2811		5082-2815 ΔV_F = 20 mV	5082-2814 ΔV_F = 20 mV	5082-2813 ΔV_F = 20 mV	5082-2826 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz
2835					5082-2080 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz



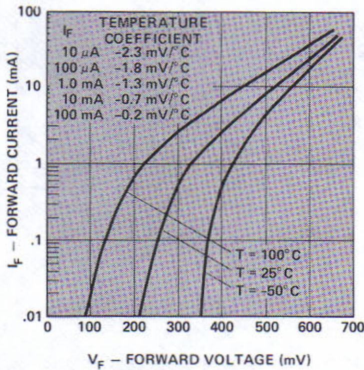


Figure 1. I-V Curve Showing Typical Temperature Variation for 5082-2300 Series Schottky Diodes.

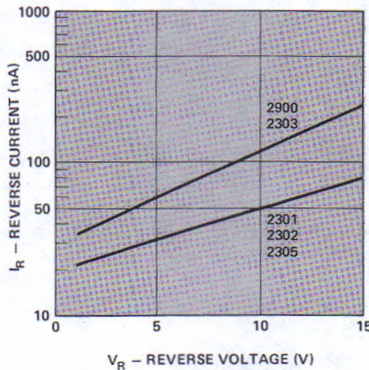


Figure 2. 5082-2300 and 5082-2900 Series Typical Reverse Current vs. Reverse Voltage at $T_A = 25°C$.

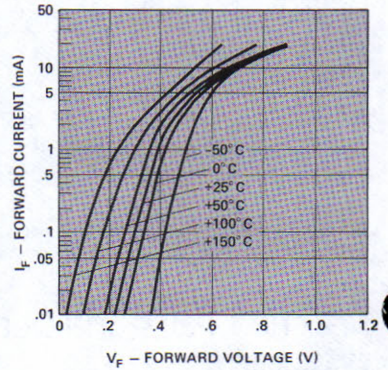


Figure 3. I-V Curve Showing Typical Temperature Variation for 5082-2800 or 1N5711 Schottky Diodes.

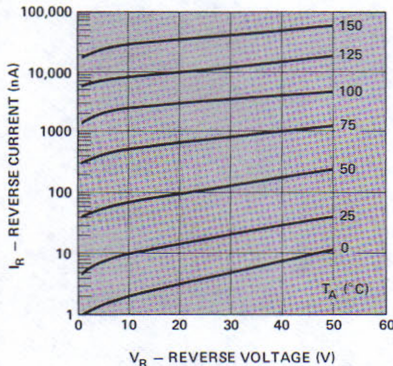


Figure 4. (5082-2800 or 1N5711) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

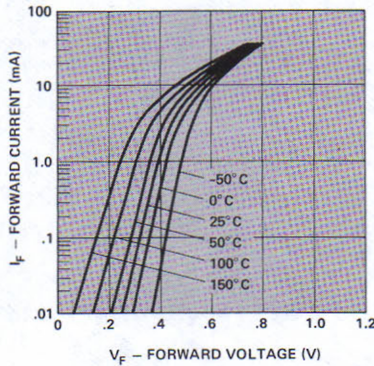


Figure 5. I-V Curve Showing Typical Temperature Variation for the 5082-2810 or 1N5712 Schottky Diode.

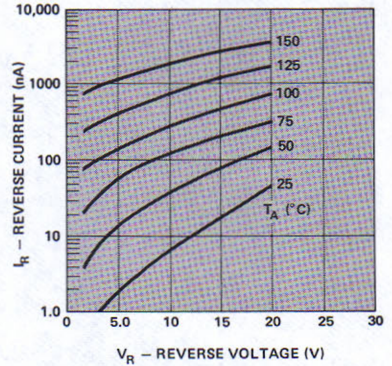


Figure 6. (5082-2810 or 1N5712) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

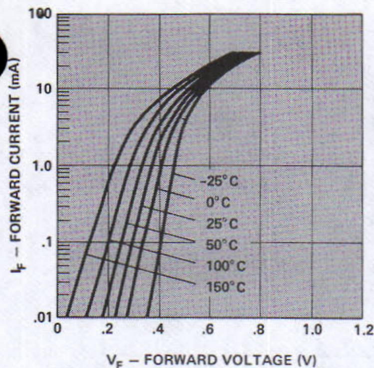


Figure 7. I-V Curve Showing Typical Temperature Variation for 5082-2811 Schottky Diode.

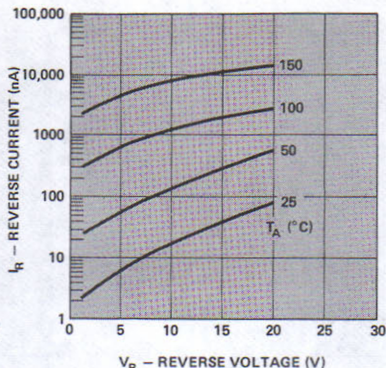


Figure 8. (5082-2811) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

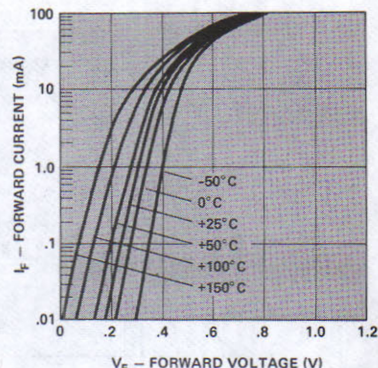


Figure 9. I-V Curve Showing Typical Temperature Variations for 5082-2835 Schottky Diode.

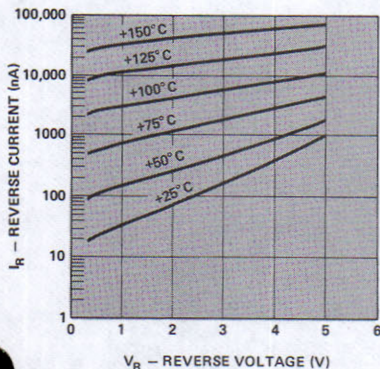


Figure 10. (5082-2835) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

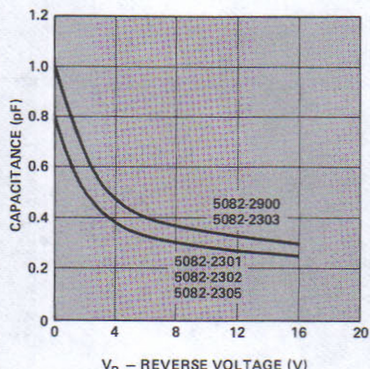


Figure 11. 5082-2300 and -2900 Series Typical Capacitance vs. Reverse Voltage.

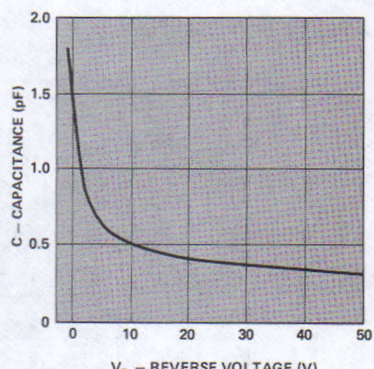


Figure 12. (5082-2800 or 1N5711) Typical Capacitance (C) vs Reverse Voltage (V_R).

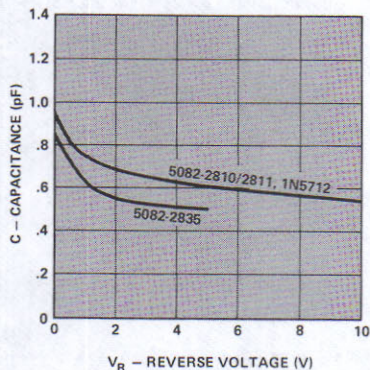


Figure 13. Typical Capacitance (C) vs. Reverse Voltage (V_R).

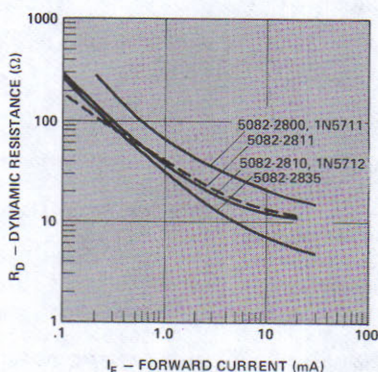


Figure 14. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

Schottky Barrier Diodes

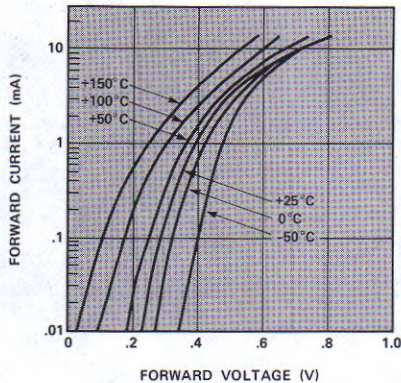


Figure 15. Typical Variation of Forward Current (I_F) vs. Forward Voltage (V_F) at Various Temperatures for the HSCH-1001.

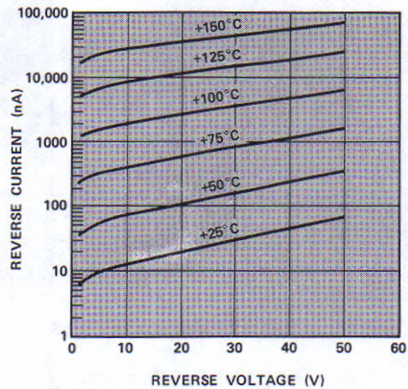


Figure 16. Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures for the HSCH-1001.

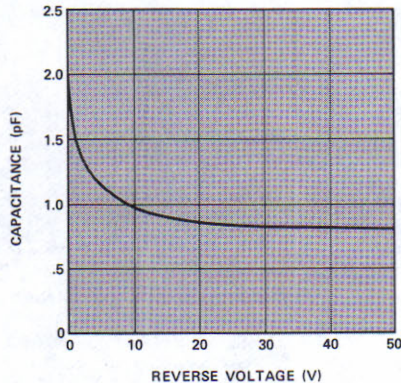


Figure 17. Typical Capacitance (C) vs. Reverse Voltage (V_R) for the HSCH-1001.

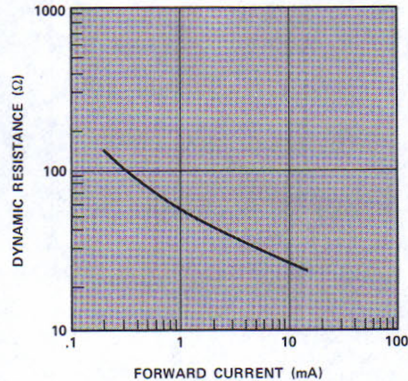
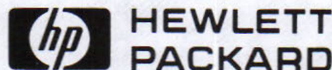


Figure 18. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F) at $T_A = 25°C$ for the HSCH-1001.

Mechanical Specifications

	Outline 15	Outline 12
Lead Material:	Dumet	Dumet
Lead Finish:	1N5711, 1N5712: Tin 2800 Series: Tin 2300, 2900 Series: Gold	Tin
Maximum Soldering Temperature:	230°C for 5 sec.	260°C for 10 sec.
Minimum Lead Strength:	4 lb. Pull	10 lb. Pull
Typical Package Inductance:	1N5711, 1N5712: 2.0 nH 2800 Series: 2.0 nH 2300, 2900 Series: 3.0 nH	1.8 nH
Typical Package Capacitance:	1N5711, 1N5712: 0.2 pF 2800 Series: 0.2 pF 2300, 2900 Series: 0.07 pF	0.25 pF

The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch from the glass body.

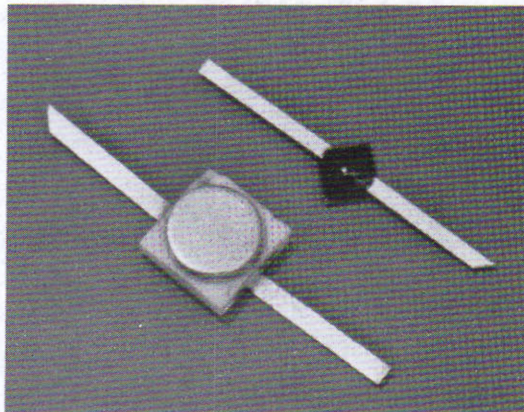


SCHOTTKY BARRIER DIODES FOR STRIPLINE, MICROSTRIP MIXERS AND DETECTORS

5082-2200/01/02/03
5082-2207/08/09/10
5082-2765/66
5082-2774/75
5082-2213-18
5082-2785/86
5082-2794/95

Features

- **SMALL SIZE**
- **LOW NOISE FIGURE**
  6 dB Typical at 9 GHz
- **RUGGED DESIGN**
- **HIGH UNIFORMITY**
- **HIGH BURNOUT RATING**
  1 W RF Pulse Power Incident
- **BOTH MEDIUM AND LOW BARRIER AVAILABLE**



Description/Applications

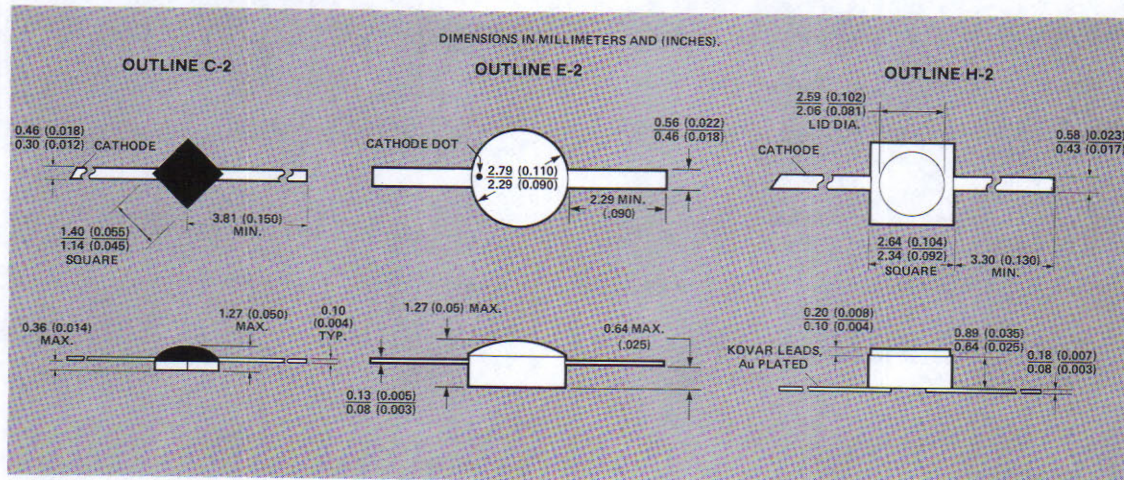
This family consists of medium barrier and low barrier beam lead diodes mounted in easily handled carrier packages. Low barrier diodes provide optimum noise figure at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. Application Note 976 presents impedance matching techniques for an X-Band mixer.

Mechanical Specifications

These diodes are designed for microstrip and stripline use. The kovar leads provide good continuity of transmission line impedance to the diode. Outlines C2 and E2 are plastic on ceramic packages. Outline H2 has a metal ceramic hermetic seal. The ceramic is alumina. Metal parts are gold plated kovar.

The hermetic package, outline H2, is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1: 260° C, 10 seconds.

Package Dimensions



RF Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Batch* Matched 5082-	Test Freq. (GHz)	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	Max.	Maximum SWR	Package	Typical Capacitance C_T (pF)
2200	2201		Medium	6.0	200	400	1.5:1		
2202	2203		Medium	6.5	200	400	2.0:1	Hermetic	
2765	2766		Low	6.0	100	250	1.5:1	H-2	0.3
2785	2786		Low	6.5	100	250	2.0:1		
2207	2208	9.375	Medium	6.0	250	500	1.5:1		
2209	2210		Medium	6.5	250	500	2.0:1	Broadband	
2774	2775		Low	6.0	200	400	1.5:1	C-2	
2794	2795		Low	6.5	200	400	2.0:1		0.22
2217	2218			6.5			1.5:1		
2213	2214	3	Medium	6.0	200	400	1.5:1	Low Cost	
2215	2216			7.0			2.0:1	E-2	
Test Conditions	ΔNF≤0.3dB ΔZ_{IF}≤25Ω			DC Load Resistance = 0Ω L.O. Power = 1 mW IF = 30 MHz, 1.5 dB NF					V = 0

*Minimum batch size 20 units.

Typical Detector Parameters

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20 μA Bias
Voltage Sensitivity	γ	6.6	mV/μW	Video Bandwidth = 2 MHz R_L = 100KΩ
Video Resistance	R_V	1400	Ω	f = 10 GHz

Note: The low barrier units are also useful at zero bias.

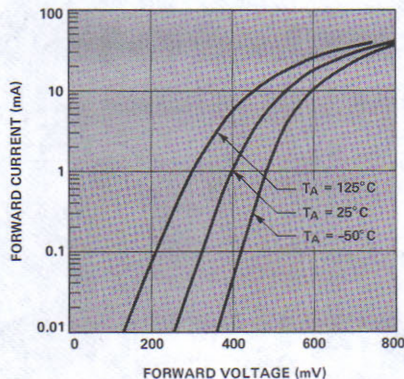


Figure 1. Typical Forward Characteristics.

MEDIUM BARRIER

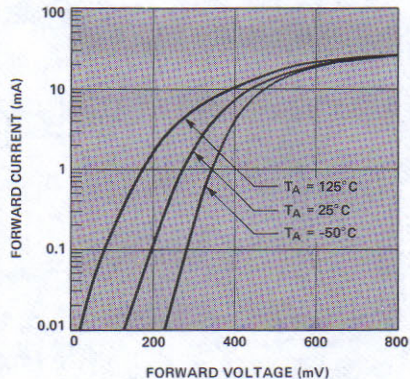


Figure 2. Typical Forward Characteristics.

LOW BARRIER

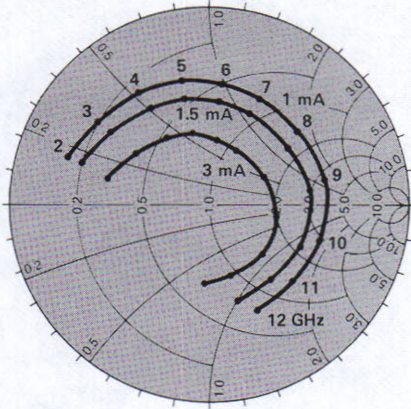


Figure 3. Typical Admittance Characteristics, 5082-2200 with self bias.

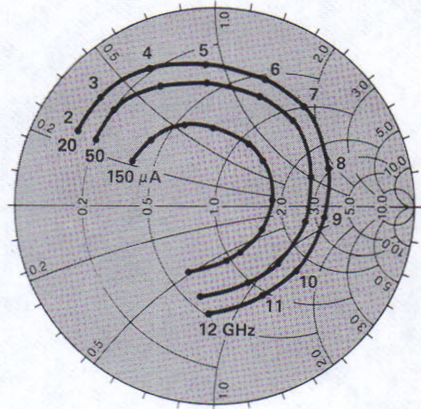


Figure 4. Typical Admittance Characteristics, 5082-2200 with external bias.

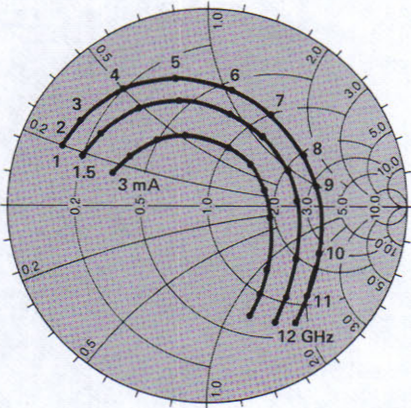


Figure 5. Typical Admittance Characteristics, 5082-2202 with self bias.

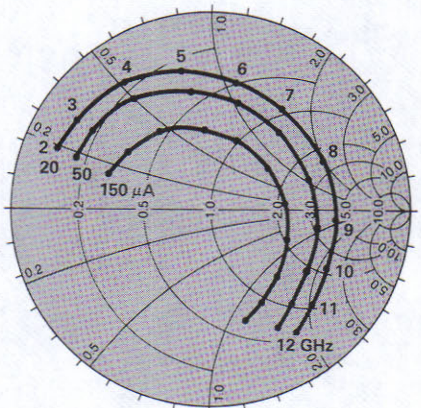


Figure 6. Typical Admittance Characteristics, 5082-2202 with external bias.

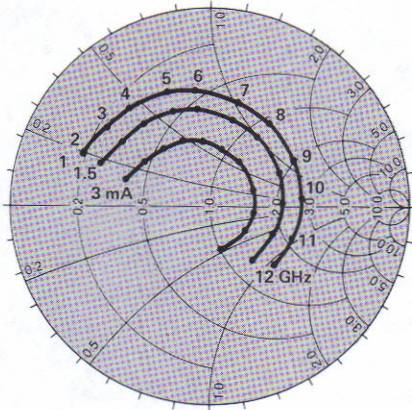


Figure 7. Typical Admittance Characteristics, 5082-2765 with self bias.

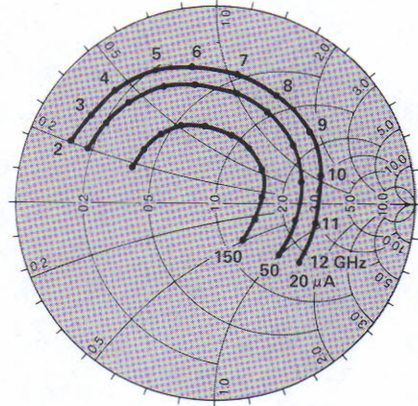


Figure 8. Typical Admittance Characteristics, 5082-2765 with external bias.

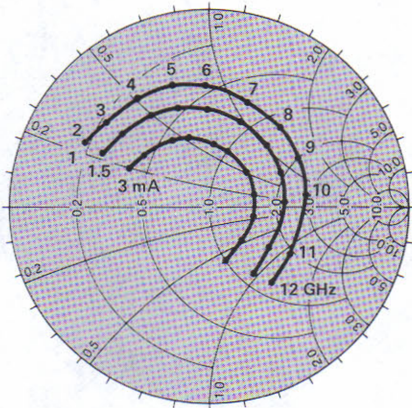


Figure 9. Typical Admittance Characteristics, 5082-2785 with self bias.

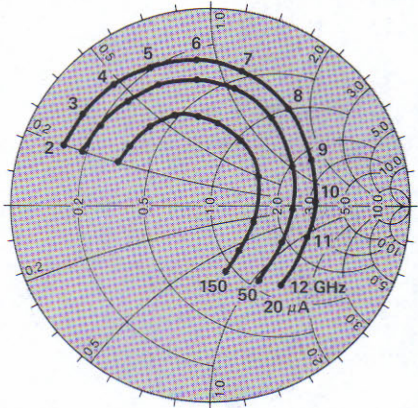


Figure 10. Typical Admittance Characteristics, 5082-2785 with external bias.

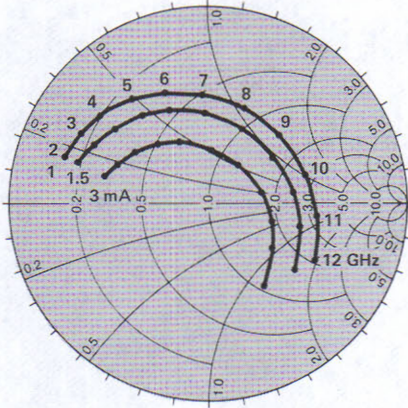


Figure 11. Typical Admittance Characteristics, 5082-2207 with self bias.

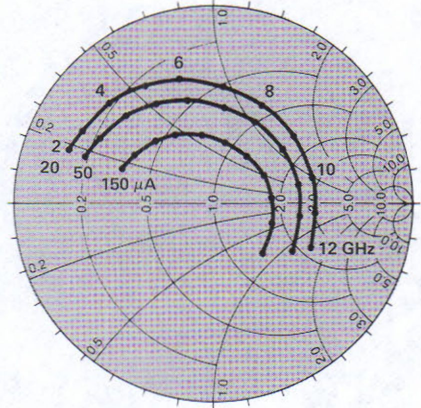


Figure 12. Typical Admittance Characteristics, 5082-2207 with external bias.

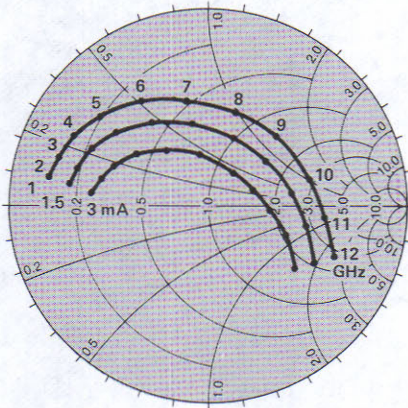


Figure 13. Typical Admittance Characteristics, 5082-2209 with self bias.

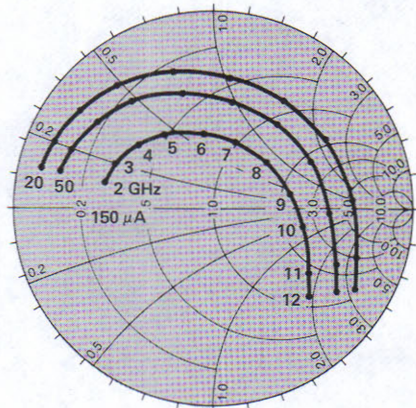


Figure 14. Typical Admittance Characteristics, 5082-2209 with external bias.

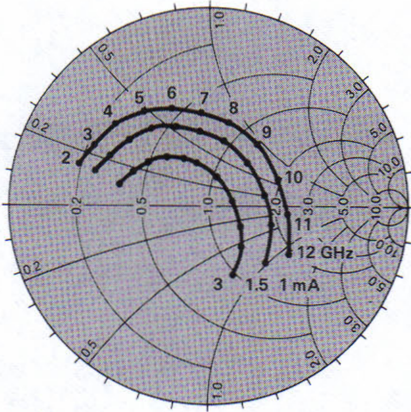


Figure 15. Typical Admittance Characteristics, 5082-2774 with self bias.

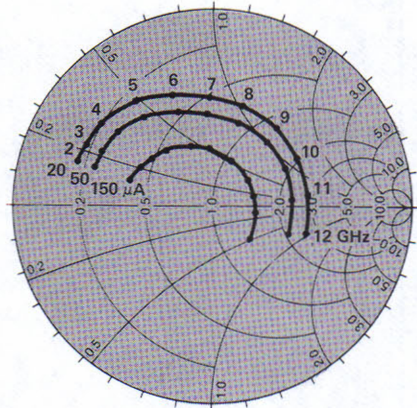


Figure 16. Typical Admittance Characteristics, 5082-2774 with external bias.

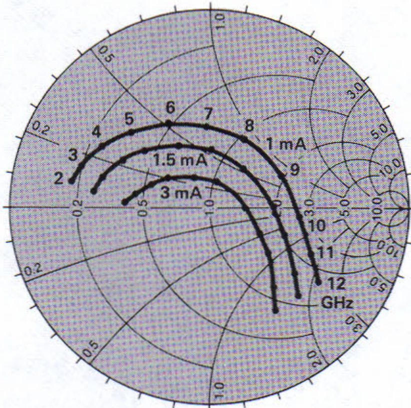


Figure 17. Typical Admittance Characteristics, 5082-2794 with self bias.

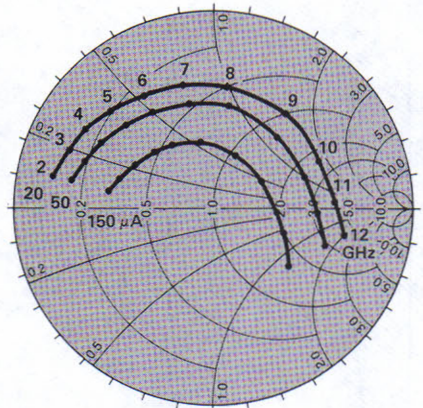


Figure 18. Typical Admittance Characteristics, 5082-2794 with external bias.

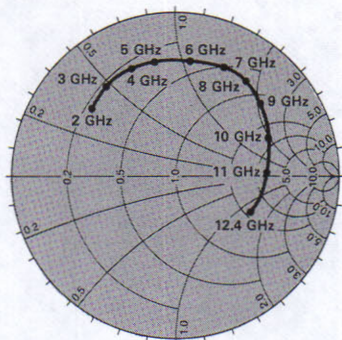


Figure 19. Typical Admittance Characteristics, 5082-2213, -2216 with self bias. Rectified current 1.0 mA.

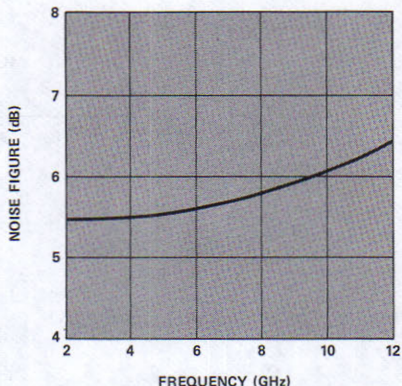


Figure 20. Typical Single Sideband Noise Figure vs. Frequency, 5082-2217.

Maximum Ratings at $T_{CASE} = 25°C$

Pulse Power Incident

- E-2 .... 0.8W
- C-2, H-2 .... 1W

(1 μs pulse, Du = .001 for 1 minute)

CW Power Dissipation

(Mounted in infinite Heat Sink) .... 125 mW

(Derate linearly to Zero at Maximum Operating Temperature)

Junction Operating and Storage Temperature Range

- E-2, C-2 Packaged Diodes .... -65°C to +125°C
- H-2 Packaged Diodes .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10⁷ hours.

Diode Mounting Temperature

- E-2 .... 220°C for 10 sec max.
- C-2 .... 235°C for 10 sec max.
- H-2 .... 260°C for 10 sec max.

Peak Inverse Voltage .... 3 V

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

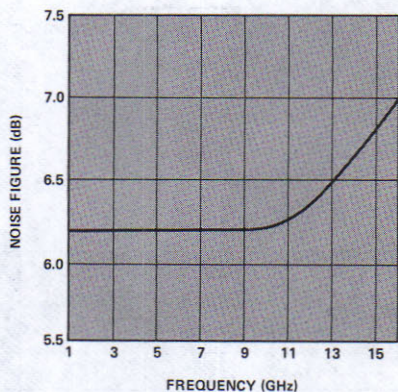


Figure 21. Typical Noise Figure vs. Frequency for 5082-2202, -2209, -2785, -2794.

PACKAGE	DIMENSION "A"
C-2	1.91 ± 0.05 (0.075 ± 0.002)
H-2 E-2	2.67 ± 0.05 (0.105 ± 0.002)

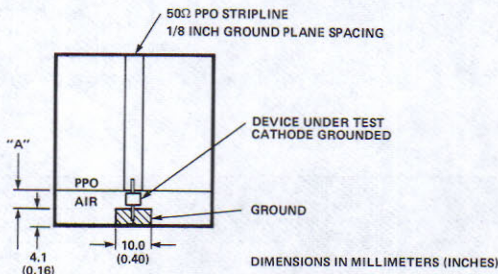
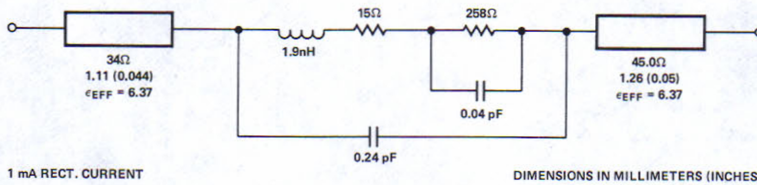


Figure 22. Admittance Test Circuit.

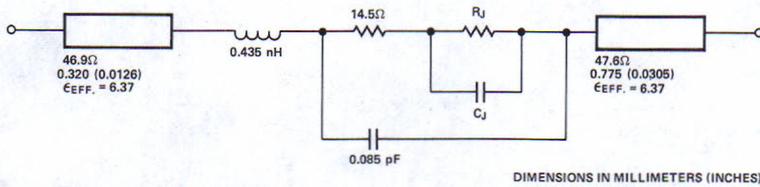
MODEL FOR E2 DIODES



1 mA RECT. CURRENT

DIMENSIONS IN MILLIMETERS (INCHES)

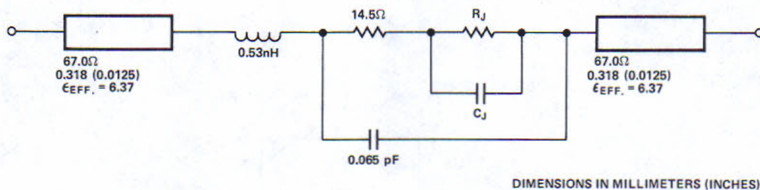
MODEL FOR H2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current		20 µA Ext. Bias		Units
		5082-2200	5082-2765	5082-2200	5082-2765	
Junction Resistance	R_J	258	290	545	495	Ohms
Junction Capacitance	C_J	0.255	0.189	0.302	0.173	pF

MODEL FOR C-2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current		20 µA Ext. Bias		Units
		5082-2207	5082-2774	5082-2207	5082-2774	
Junction Resistance	R_J	338	255	421	340	Ohms
Junction Capacitance	C_J	0.189	0.180	0.195	0.168	pF

HEWLETT PACKARD

SCHOTTKY BARRIER DIODE QUADS FOR DOUBLE BALANCED MIXERS

5082-2231
5082-2233
5082-2263
5082-2271/72
5082-2277
5082-2279/80
5082-2291/92
5082-2294
5082-2830/31

Features

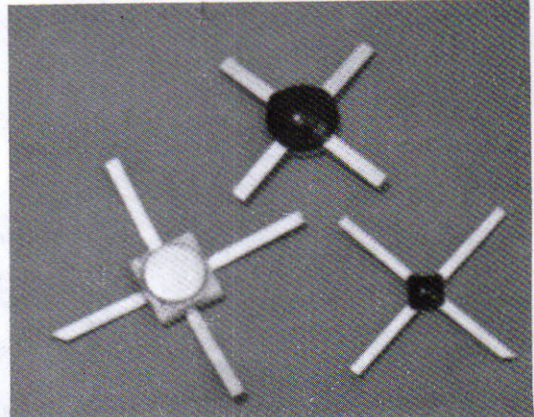
SMALL SIZE
Eases Broad Band Designs

TIGHT MATCH
Improves Mixer Balance

IMPROVED BALANCE OVER TEMPERATURE

RUGGED DESIGN

BOTH MEDIUM AND LOW BARRIER DIODES AVAILABLE



Description / Applications

These matched diode quads use a monolithic array of Schottky diodes interconnected in ring configuration. The relative proximity of the diode junction on the wafer assures uniform electrical characteristics and temperature tracking.

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size. The low barrier diodes allow for optimum mixer noise figure at lower than conventional local oscillator levels. The wider dynamic range of the medium barrier diodes allows for better distortion performance.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range:
H-4 Packaged Diodes .... -65°C to +150°C
E-1 and C-4 Packaged Diodes .... -65°C to +125°C

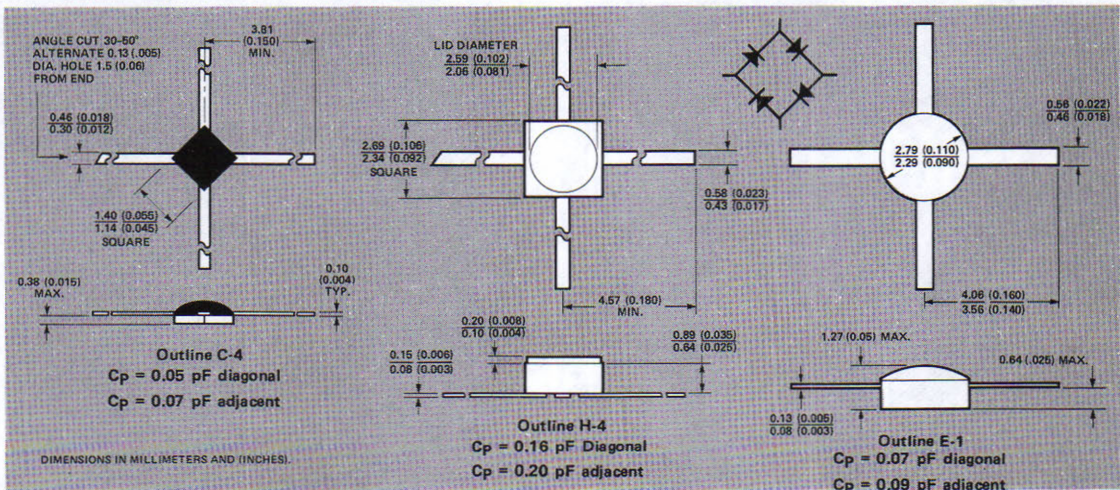
Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

DC Power Dissipation .... 75 mW per Junction
Derate linearly to zero at maximum rated temperatures (measured in infinite heat sink)

Soldering Temperature .... H-4 260° C for 10 sec.
C-4 235° C for 10 sec.
E-1 220° C for 10 sec.

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

Package Dimensions



Outline C-4
Cp = 0.05 pF diagonal
Cp = 0.07 pF adjacent

Outline H-4
Cp = 0.16 pF Diagonal
Cp = 0.20 pF adjacent

Outline E-1
Cp = 0.07 pF diagonal
Cp = 0.09 pF adjacent

Selection Guide

Package Outline \ Frequency	Barrier	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
E-1	Medium	5082-2830	5082-2277	5082-2277		
Low Cost	Low	5082-2831				
H-4	Medium	5082-2263	5082-2263	5082-2263		
Hermetic	Low	5082-2231	5082-2231	5082-2233		
C-4	Medium	5082-2291	5082-2291	5082-2292	5082-2294	5082-2294
Broadband	Low	5082-2271	5082-2271	5082-2272	5082-2279	5082-2280

Electrical Characteristics at $T_A = 25°C$ / Typical Parameters

Part Number 5082-	Package	Barrier	Maximum Capacitance C_T (pF)	Maximum Capacitance Difference ΔC_T (pF)	Maximum V_F Difference ΔV_F (mV)	Maximum Dynamic Resistance R_D (Ω)	Typical Parameters: Forward Voltage V_F (V)
2231	H-4	Low	0.60	0.10	20	12	0.25
2233			0.40	0.05		16	0.30
2263		Medium	0.40	0.05		16	0.45
2830	E-1		0.5 Typ.	0.20		12	0.40
2831		Low	0.5 Typ.	0.20		12	0.25
2277		Medium	0.50	0.10		15	0.35
2271	C-4	Low	0.60	0.10		12	0.25
2272			0.45	0.10		15	0.25
2279			0.25	0.05		16	0.30
2280			0.20	0.05		16	0.30
2291		Medium	0.60	0.10		12	0.35
2292			0.40	0.10		15	0.35
2294			0.20	0.05		16	0.45
Test Conditions			$V_R = 0$, f = 1 MHz[1]		$I_F = 5mA$ between Adjacent Leads		$I_F = 1mA$ Measured between Adjacent Leads

Note: 1. Measured between diagonal leads.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. The two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B \quad \text{where}$$

I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Package Characteristics

The HP outline E1 package is designed for MIC, Microstrip, and Stripline use from dc through X-Band. The leads provide a good continuity of transmission line impedance to the monolithic diode array.

The C-4 subminiature package is a ceramic carrier whose gold plated kovar leads are brazed to the substrate for maximum package ruggedness. If the leads are to be formed, they should be restricted so the bend starts at least 0.25 mm (0.01 inch) from the package body. The semiconductor is protected from mechanical abrasion by a junction coating. The H-4 miniature package is a hermetic metal-ceramic device, which makes it ideal for applications requiring high reliability. The leads are gold plated kovar. Outline H-4 is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1:260° C, 10 seconds.

HEWLETT PACKARD

SCHOTTKY BARRIER DIODES FOR MIXERS AND DETECTORS

5082-2273/74
5082-2295-98
5082-2350/51
5082-2400/01
5082-2520/21/65/66
5082-2701/02/06/07
5082-2711-14/23-24
5082-2817/18

Schottky Barrier Diodes

Features

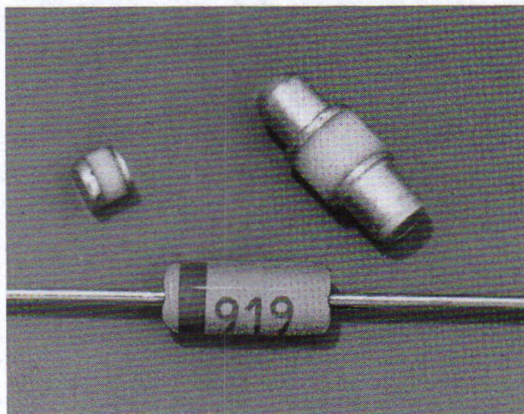
LOW AND STABLE NOISE FIGURE

HIGH BURNOUT RATING
15 W RF Pulse Power Incident

RUGGED DESIGN

HIGH UNIFORMITY

BOTH MEDIUM AND LOW BARRIER DIODES AVAILABLE



Description / Applications

These Schottky diodes are optimized for use in broad band and narrow band microstrip, coaxial, or waveguide mixer assemblies operating to 18 GHz. The low barrier diodes give optimum noise figure performance at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. The 5082-2350, -2400, -2520 and -2565 have extremely low 1/f noise, making them ideal for use as Doppler mixers.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range
5082-2400, 2401, 2565, 2566, 2350, 2351, 2520, 2521 .... -60° C to +125° C
All other diodes .... -60° C to +150° C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

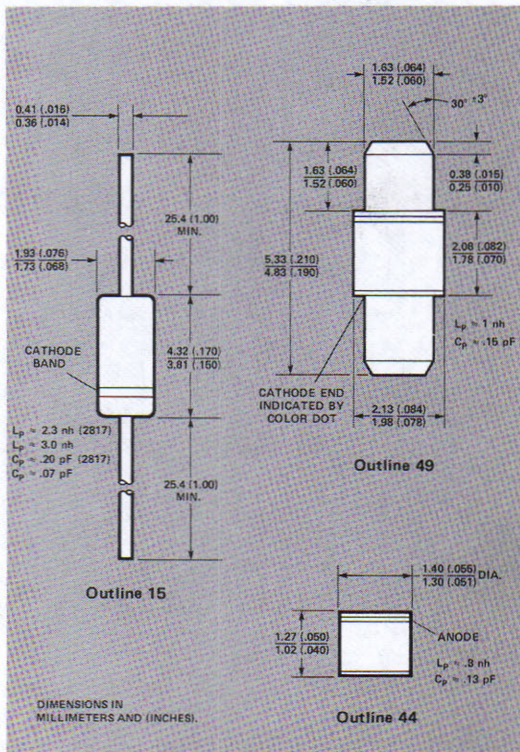
CW Power Dissipation .... 200 mW
Derate linearly to 0 W at max. rated temperature (Measured in an infinite heat sink).

Pulse Power Dissipation
Peak power absorbed by the diode.
1 μs pulse, Du = .001 .... 1W

Soldering Temperature .... 230° C for 5 sec.

Note: The 5082-2200, -2500 and -2700 series are pulse sensitive. Handle with care to avoid static discharge through the diode.

Package Dimensions



Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Matched Pair 5082-	Barrier	LO Test Frequency (GHz)	Maximum SSB Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Package Outline
2817	2818	Medium	2.0	6.0	250	400	1.5:1	
2400	2401	Medium	2.0	6.0	150	250	1.3:1	
2350	2351	Medium	2.0	7.0	150	250	1.5:1	15
2565	2566	Medium	3.0	6.0	100	250	1.5:1	
2520	2521	Medium	3.0	7.0	100	250	1.5:1	
2713	2714	Medium	9.375	6.0	200	400	1.5:1	49
2711	2712	Medium	9.375	6.5	200	400	2.0:1	
2701	2706	Medium	9.375	6.0	200	400	1.5:1	
2702	2707	Medium	9.375	6.5	200	400	1.5:1	44
2295	2296	Low	9.375	6.0	100	250	1.5:1	
2297	2298	Low	9.375	6.5	100	250	2.0:1	
2723	2724	Medium	16	6.5	200	400	1.5:1	49
2273	2274	Medium	16	6.5	200	400	1.5:1	44
Test Conditions	$\Delta NF \leq 0.3dB$ $\Delta Z_{IF} \leq 25\Omega$		LO Power = 1 mW IF=30 MHz, 1.5 dB NF Zero DC Load Resistance (100Ω for 5082-2817)		Same as for NF except IF = 10 KHz		Same as for NF	

Typical Parameters

Part Number 5082-	Junction Capacitance C_{JO} (pF)	Breakdown Voltage V_{BR} (V)
2817	1.0	15
2400	0.7	30
2350	0.9	30
2565	0.5	5
2520	0.7	5
2713		
2711		
2701		4
2702		
2295	0.10	
2297		
2723		3
2273		3
Test Conditions	V = 0	$I_R = 10\ \mu A$

Typical Parameters

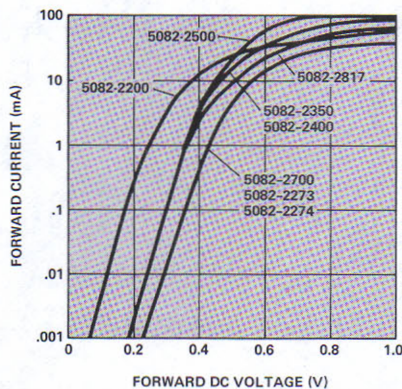


Figure 1. Typical Forward Characteristics at $T_A = 25°C$.

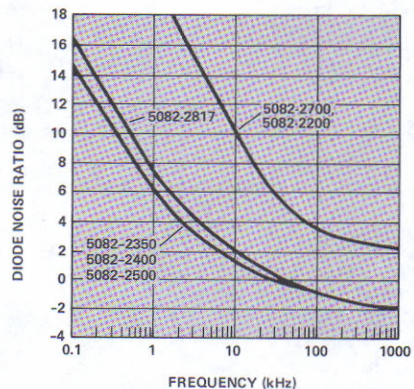


Figure 2. Typical Diode Noise Ratio vs. Frequency at 1 mA Current.

Package Characteristics

The HP Outline 15 package has a glass hermetic seal with plated Dumet leads which should be restricted so that the bend starts at least 1/16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750. Method 2036, Conditions A and E (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud T/R is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230° C for 5 seconds.

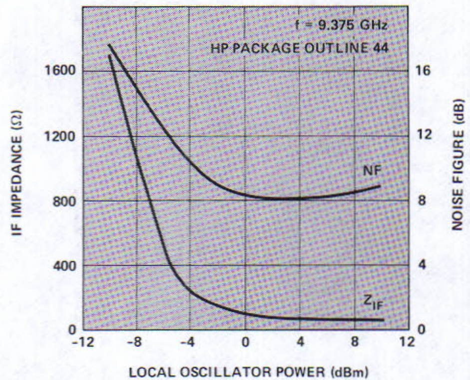


Figure 3. Typical Noise Figure and IF Impedance vs. Local Oscillator Power, 5082-2295 through -2298. Diode unmatched in 50Ω line.

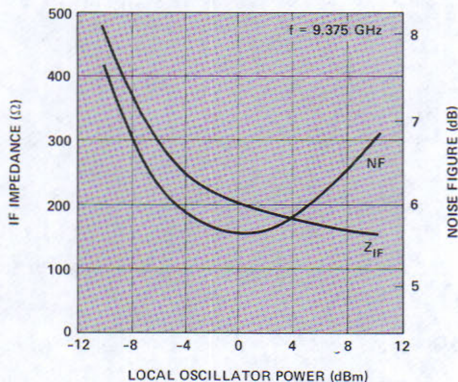


Figure 4. Typical Noise Figure and IF Impedance vs. Local Oscillator Power. Diode matched at each local oscillator power level (5082-2295).

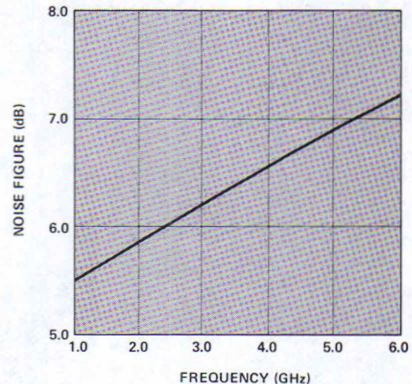


Figure 5. Typical HP 5082-2400 Noise Figure vs. Frequency with P_{LO} = 1.0 mW, f_{IF} = 30 MHz, and NF_{IF} = 1.5 dB. Mount tuned at each frequency.

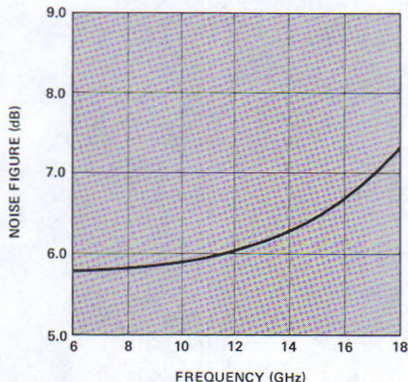


Figure 6. Typical Noise Figure vs. Frequency. IF = 30 MHz, NF_{IF} = 1.5 dB, P_{LO} = 1 mW. Diode matched at each frequency (5082-2200, 2700 series).

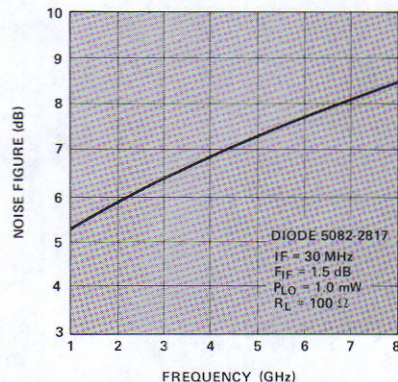


Figure 7. Typical Noise Figure vs. Frequency. The mount is tuned for minimum noise figure at each frequency.

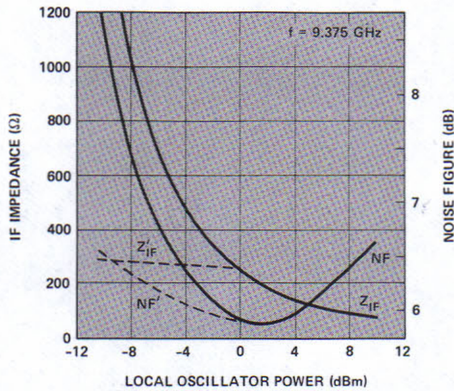


Figure 8. Typical Noise Figure and IF Impedance for 5082-2711 vs. Local Oscillator Power. Note the improved performance at low levels of LO power when dc bias is superimposed (dashed curves).

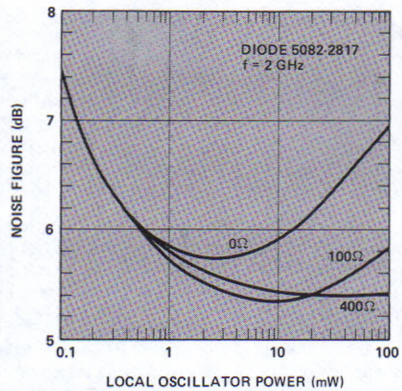


Figure 9. Single Sideband Noise Figure (including an IF-amplifier noise figure of 1.5 dB) vs. Incident LO Power for Various dc-load Resistances R_L. (The mount is tuned for minimum noise figure at each LO power level).

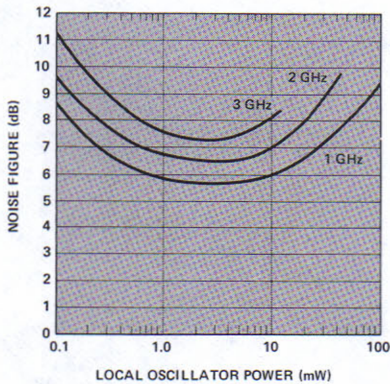


Figure 10. Typical 5082-2350 Noise Figure vs. Local Oscillator Power at 1.0, 2.0 and 3.0 GHz with IF = 30 MHz and NF_{IF} = 1.5 dB.

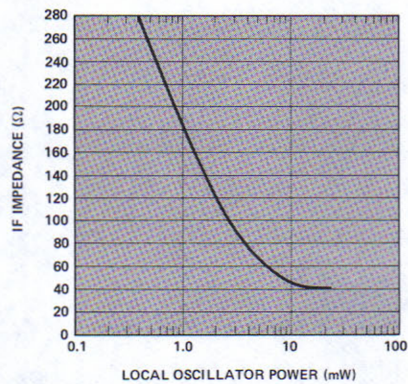


Figure 11. Typical 5082-2300 and 2400 Series IF Impedance vs. Local Oscillator Power with f_{LO} = 2.0 GHz and IF = 30 MHz.

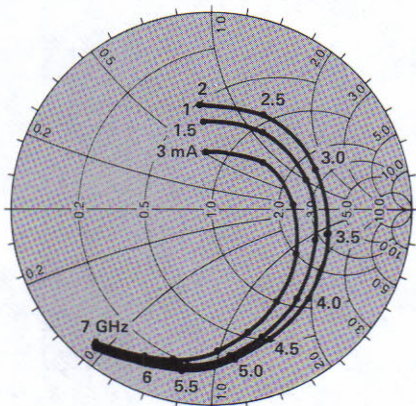


Figure 12. Typical Admittance Characteristics, 5082-2817 with self bias.

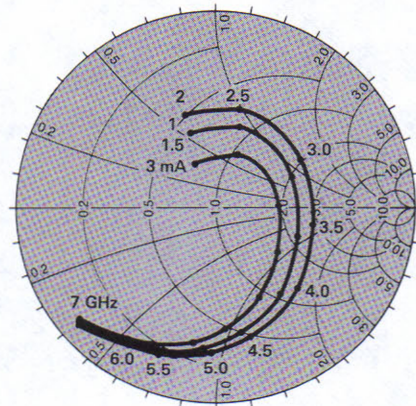


Figure 13. Typical Admittance Characteristics, 5082-2400 with self bias.

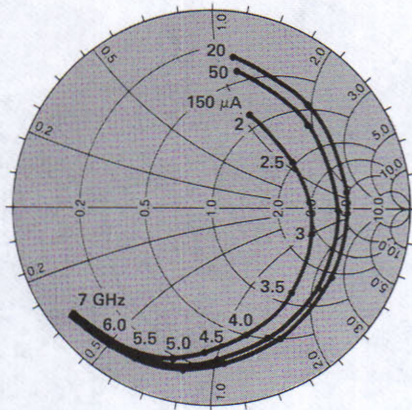


Figure 14. Typical Admittance Characteristics, 5082-2400 with external bias.

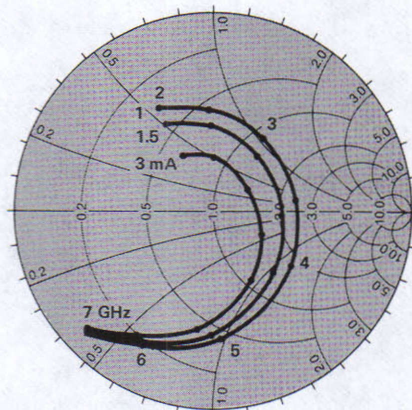


Figure 15. Typical Admittance Characteristics, 5082-2350 with self bias.

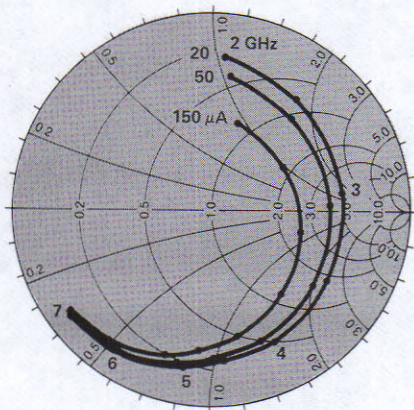


Figure 16. Typical Admittance Characteristics, 5082-2350 with external bias.

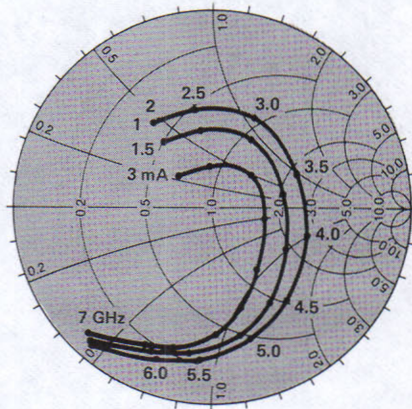


Figure 17. Typical Admittance Characteristics, 5082-2565 with self bias.

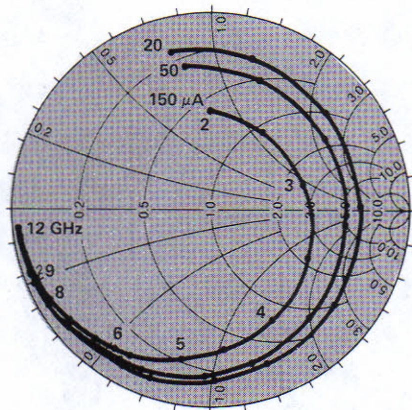


Figure 18. Typical Admittance Characteristics, 5082-2565 with external bias.

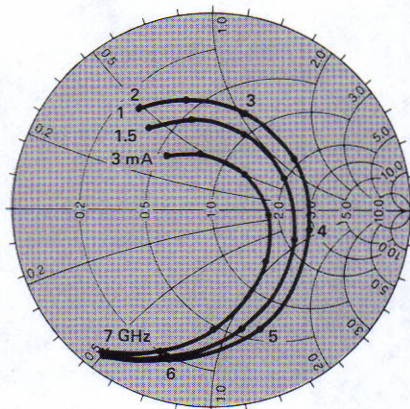


Figure 19. Typical Admittance Characteristics, 5082-2520 with self bias.

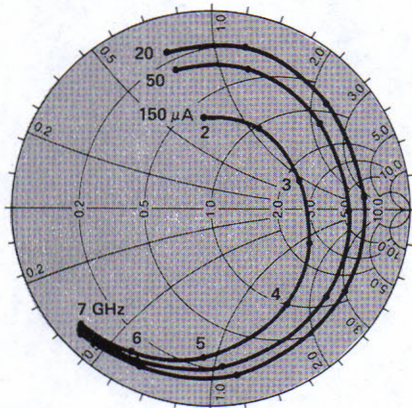


Figure 20. Typical Admittance Characteristics, 5082-2520 with external bias.

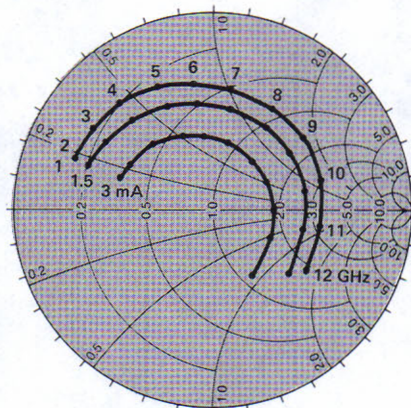


Figure 21. Typical Admittance Characteristics, 5082-2713 with self bias.

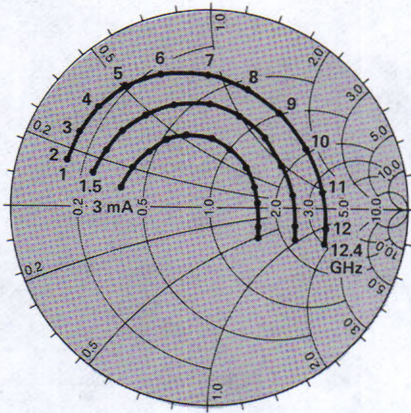


Figure 22. Typical Admittance Characteristics, 5082-2711 with self bias.

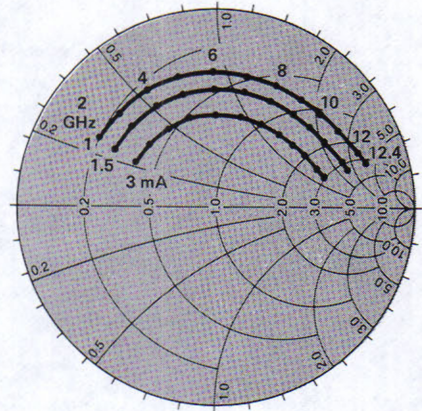


Figure 23. Typical Admittance Characteristics, 5082-2701 with self bias.

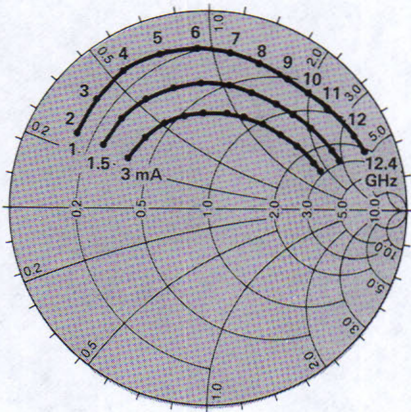


Figure 24. Typical Admittance Characteristics, 5082-2702 with self bias.

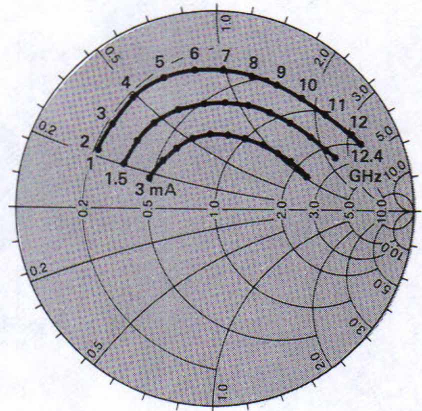


Figure 25. Typical Admittance Characteristics, 5082-2295 with self bias.

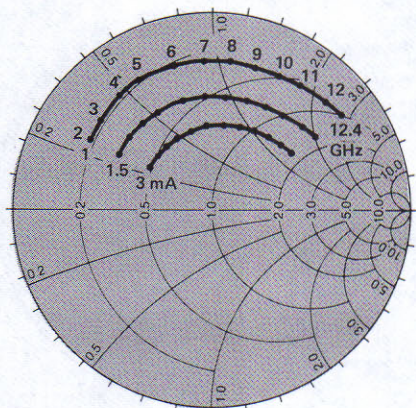


Figure 26. Typical Admittance Characteristics, 5082-2297 with self bias.

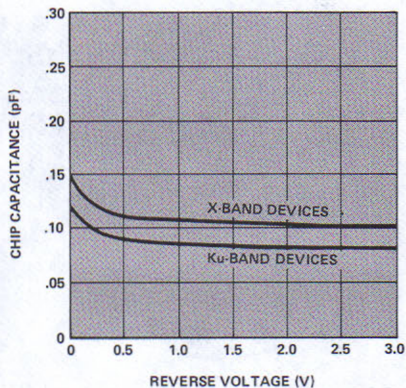


Figure 27. Typical Chip Capacitance vs. Reverse Voltage, 2700 Series.

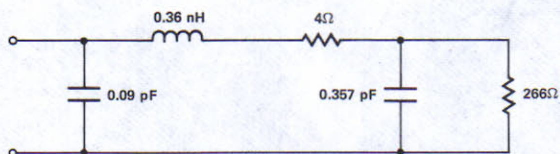
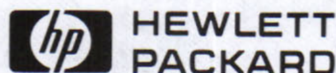


Figure 28. Model for 5082-2701 Mixer Diodes — Rectified Current 1.0 mA.



ZERO BIAS SCHOTTKY DETECTOR DIODES

HSCH-3171
HSCH-3206/07
HSCH-3486
HSCH-5018/19

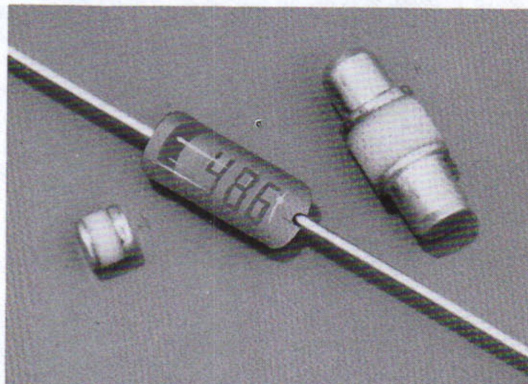
Schottky Barrier Diodes

Features

HIGH VOLTAGE SENSITIVITY

NO BIAS REQUIRED

CHOICE OF HIGH OR LOW VIDEO IMPEDANCE



Description/Applications

The high zero bias voltage sensitivity of these Schottky Barrier diodes makes them ideally suitable for narrow bandwidth video detectors, ECM receivers, and measurement equipment. These diodes also make excellent mixers for use with low power LO.

Maximum Ratings at $T_A = 25°C$

Operating Temperature .... -65° C to +150° C
Storage Temperature .... -65° C to +150° C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

Part Number HSCH-	CW Power Dissipation[1] (mW)	Peak Pulse Power Incident[2] (W)
3486	300	1
5018	500	2
5019	500	3
3171	150	0.5
3207	200	1
3206	200	1

Notes:
1. Derate linearly to zero at 150° C.
2. Pulse width = 1 microsecond. Duty cycle = 0.001.

Electrical Specifications at $T_A = 25°C$

Part Number	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Minimum Voltage Sensitivity γ (mV/μW)	Video Resistance R_V (KΩ) Min.	Max.	Typical Total Capacitance C_T (pF)
HSCH-3171	15	-48	15	80	300	0.25
HSCH-3207	44	-42	8	80	300	0.30
HSCH-3206	49	-42	10	100	300	0.30
HSCH-3486	15	-54	7.5	2	8	0.30
HSCH-5018	44	-53	7	2	8	0.40
HSCH-5019	49	-54	7	2	8	0.42
Test Conditions		Video Bandwidth = 2 MHz f_{test} = 10 GHz	Power in = -40 dBm f_{test} = 10 GHz			V_R = 0 V f = 1 MHz

Note: For HSCH-3171, -3207, -3206, I_R = 10 μA (max) at V_R = 3V at T_A = 25° C. For reverse characteristics of HSCH-3486, -5018, -5019 see Figure 3.

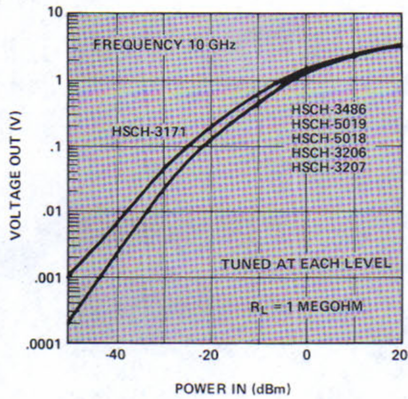


Figure 1. Typical Dynamic Transfer Characteristics.

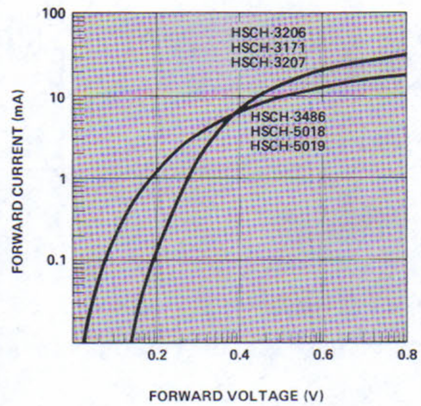


Figure 2. Typical Forward Characteristics at T_A = 25°C.

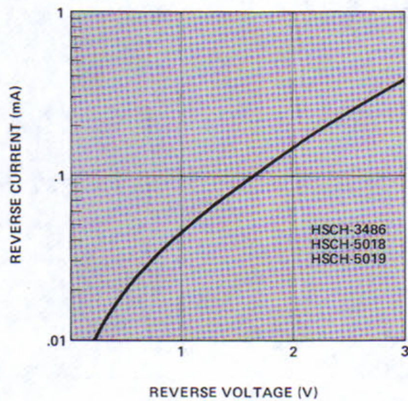


Figure 3. Typical Reverse Characteristics at T_A = 25°C.

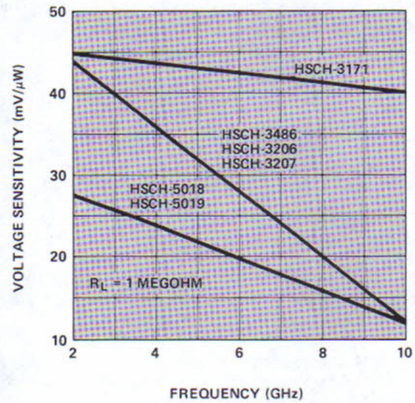


Figure 4. Typical Voltage Sensitivity vs. Frequency.

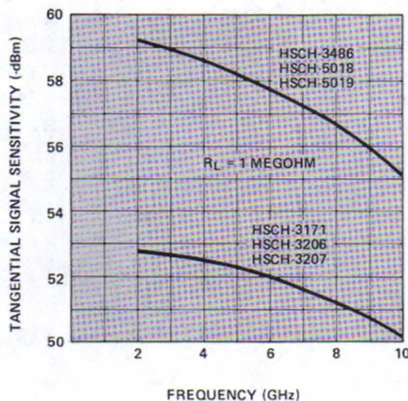


Figure 5. Typical Tangential Sensitivity vs. Frequency.

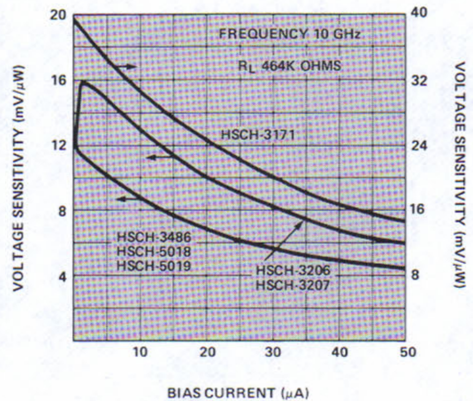


Figure 6. Typical Voltage Sensitivity vs. Bias Current.

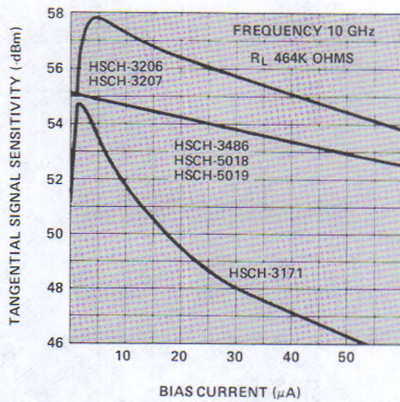


Figure 7. Typical Tangential Sensitivity vs. Bias Current.

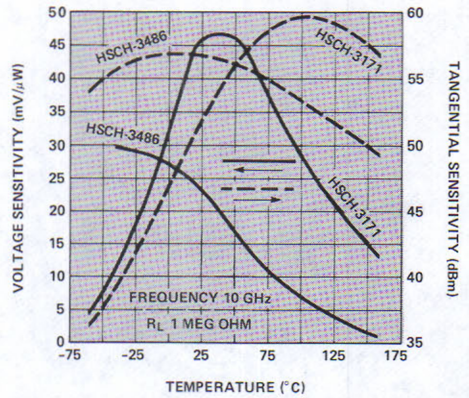


Figure 8. Effect of Temperature.

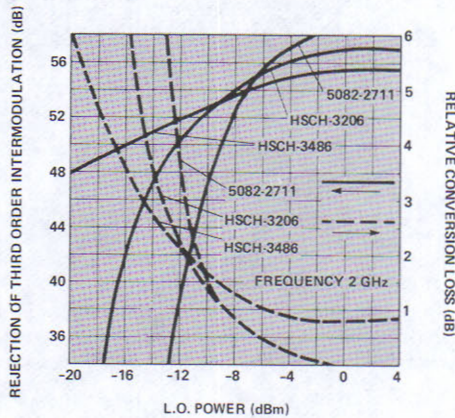


Figure 9. Mixer Performance.

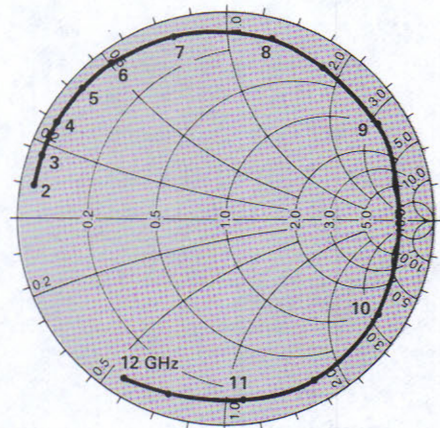


Figure 10. Typical Admittance Characteristics. HSCH-3171.

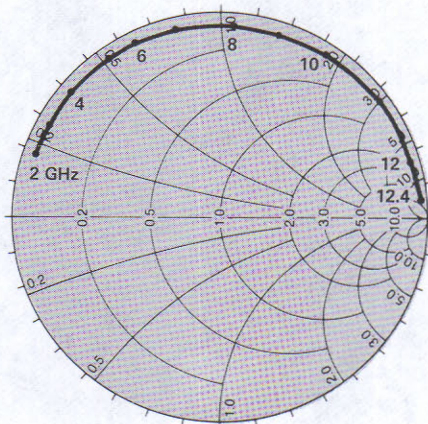


Figure 11. Typical Admittance Characteristics, HSCH-3206.

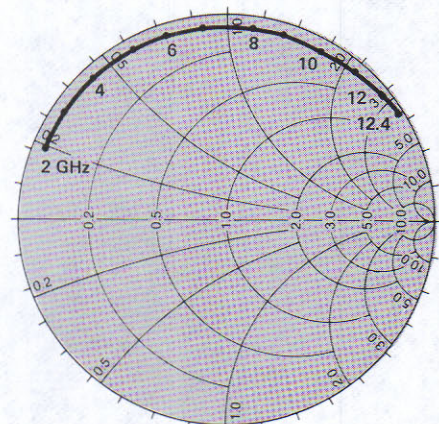


Figure 12. Typical Admittance Characteristics, HSCH-3207.

Schottky Barrier Diodes

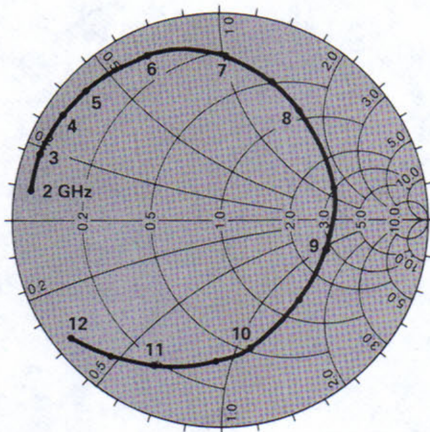
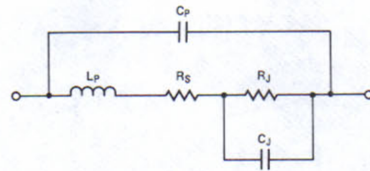


Figure 13. Typical Admittance Characteristics, HSCH-3486.



DIODE MODEL

Parameter	Symbol	Units	HSCH-3486	HSCH-3171
Package Capacitance	C_P	pF	0.063	0.060
Package Inductance	L_P	nH	2.23	2.28
Series Resistance	R_S	Ω	10	4.13
Junction Resistance	R_J	Ω	4588	171K
Junction Capacitance	C_J	pF	0.148	0.12

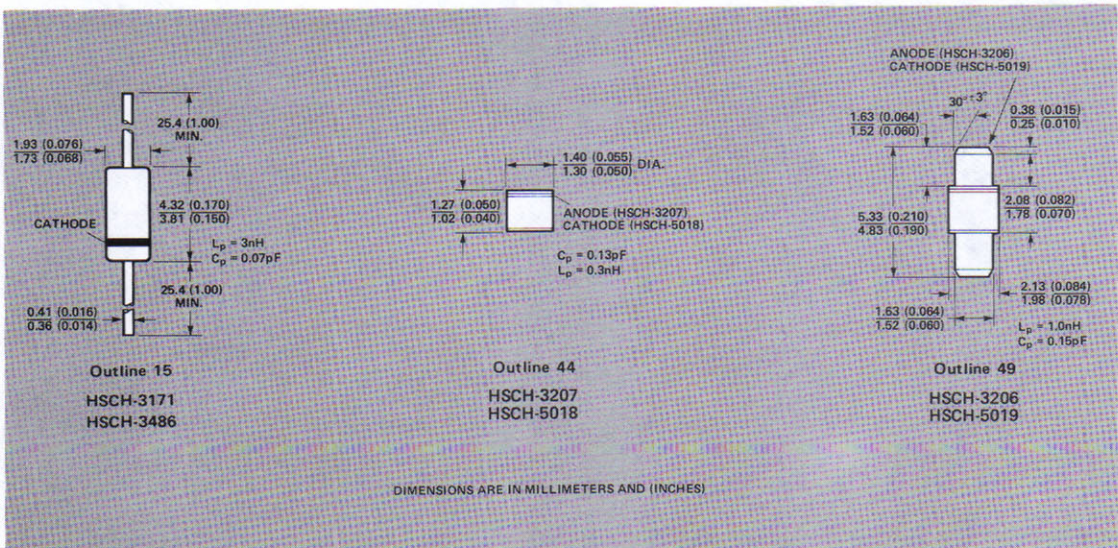
Package Characteristics

The HP Outline 15 package has a glass hermetic seal with gold plated Dumet leads which should be restricted so that the bend starts at least 1/16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Conditions A and E (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud T/R is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

Package Dimensions



HEWLETT
PACKARD

SCHOTTKY BARRIER DIODES FOR DETECTORS

5082-2750/51
5082-2755
5082-2787
5082-2824

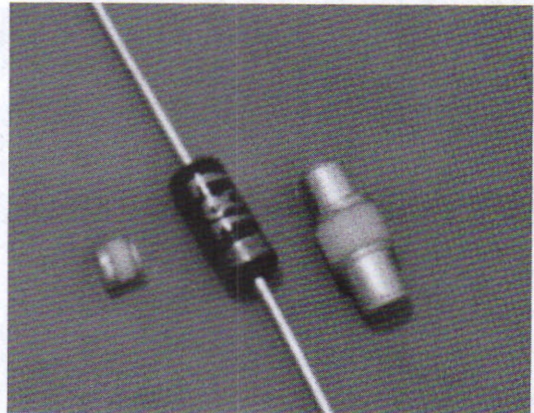
Schottky Barrier Diodes

Features

IMPROVED DETECTION SENSITIVITY
TSS OF -55 dBm at 10 GHz

LOW 1/f NOISE
Typical Noise-Temperature Ratio = 4 dB at 1 kHz

HIGH PEAK POWER DISSIPATION
4.5 W RF Peak Pulse Power



Description / Applications

The low 1/f noise and high voltage sensitivity make these Schottky barrier diodes ideally suitable for narrow bandwidth video detectors, and Doppler mixers as required in Doppler radar equipment, ECM receivers, and measurement equipment.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range
- 5082-2824 .... -65°C to +200°C
- All Others .... -60°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

DC Power Dissipation — Power Absorbed by Diode
Derate Linearly to zero at Maximum Temperature
- 5082-2824 (Applied for 1 minute) .... 1 W
- 5082-2824 (Continuous) .... 250 mW
- All Others (Continuous) .... 100 mW

Soldering Temperature .... 230°C for 5 sec.

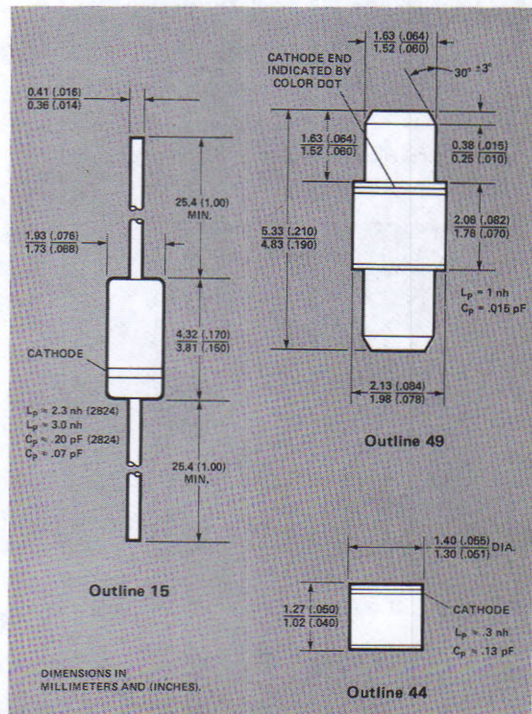
RF Peak Pulse Power
Pulse Width = 1 µs, Du = .001, R_L = 38KΩ
(Applied for 1 minute)
- 5082-2824 (Power Absorbed by Diode) ..... 4.5 W
- All Others (Power Incident) .... 2.0 W

Maximum Peak Inverse Voltage (PIV) .... V_{BR}

Note: The 2700 series diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

Package Dimensions

See Package Characteristics



Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Voltage Sensitivity Minimum γ (mV/μW)	Video Resistance R_V (kΩ) Min.	Video Resistance R_V (kΩ) Max.	Minimum Breakdown Voltage V_{BR} (V)
2824		-56	6.0		1.5	15
2787*	15	-52	3.5	1.2	1.8	
2755						4
2751	49	-55	5		1.6	
2750	44					
Test Conditions		Video Bandwidth = 2 MHz f_{RF} = 2 GHz for 5082-2824, 10 GHz for all others I_{BIAS} = 20 μA; Video Amp. Eq. Noise, R_A = 500Ω.	Same as for TSS at RF Signal Power Level of -40 dBm. Load Resistance = 100kΩ			I_R = 10 μA

Typical Parameters

Noise Temperature Ratio at f (dB)	Junction Capacitance C_{JO} (pF)
2 at 20 kHz 8 at 1 kHz	1.0
	.12
5.0 at 20 kHz 15.0 at 1 kHz	.1
R_V = 50Ω	V = 0

*RF Parameters for the 5082-2787 are sample tested only.

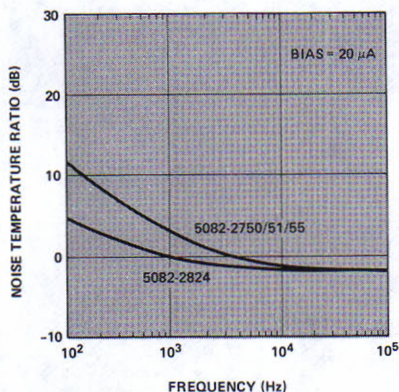


Figure 1. Typical Flicker (1/f) Noise vs. Frequency.

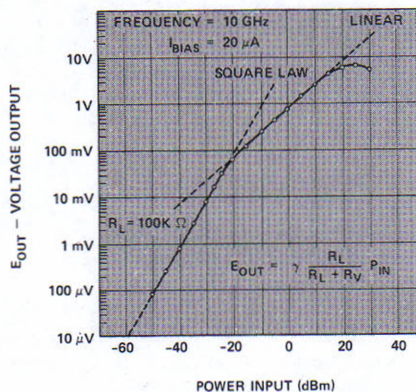


Figure 2. Typical Dynamic Transfer Characteristic. (5082-2750 Series).

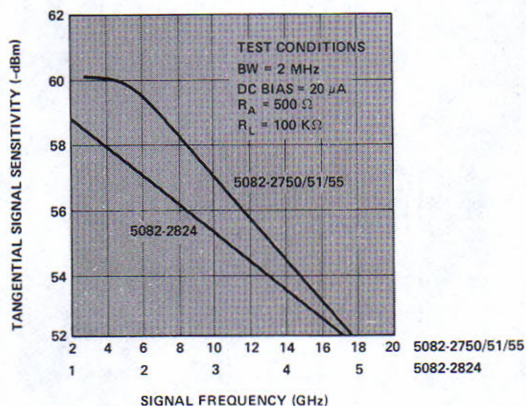


Figure 3. Typical TSS vs. Frequency.

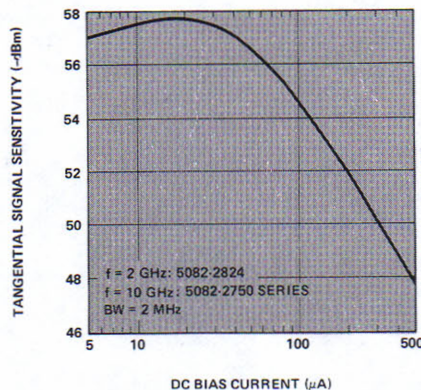


Figure 4. Typical TSS vs. Bias.

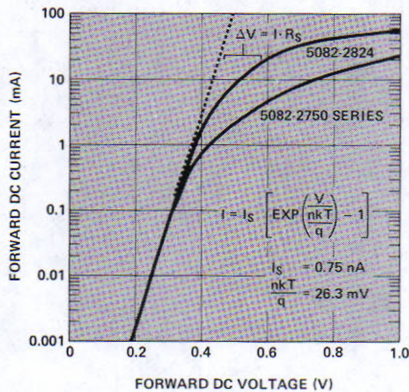


Figure 5. Typical Forward Characteristics at $T_A = 25°C$.

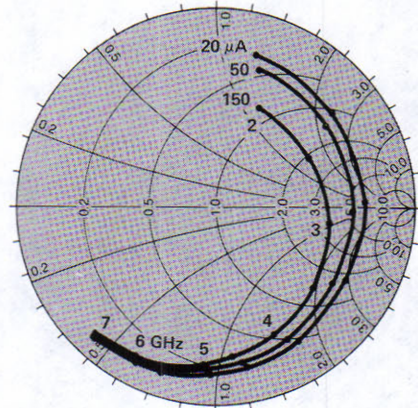


Figure 6. Typical Admittance Characteristics, 5082-2824 with external bias.

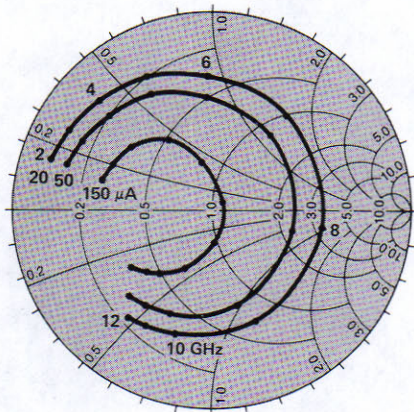


Figure 7. Typical Admittance Characteristics, 5082-2755 with external bias.

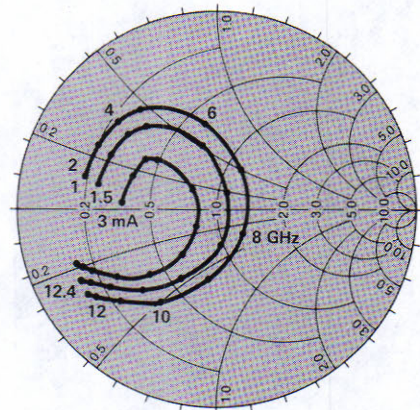


Figure 8. Typical Admittance Characteristics, 5082-2755 with self bias.

Package Characteristics

The HP Outline 15 package has a glass hermetic seal with plated Dumet leads which should be restricted so that the bend starts at least 1.16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Conditions A and E (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud T/R is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

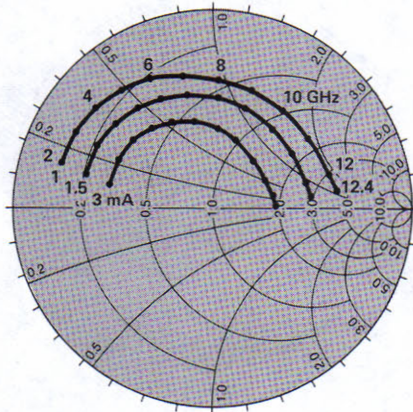


Figure 9. Typical Admittance Characteristics, 5082-2751 with self bias.

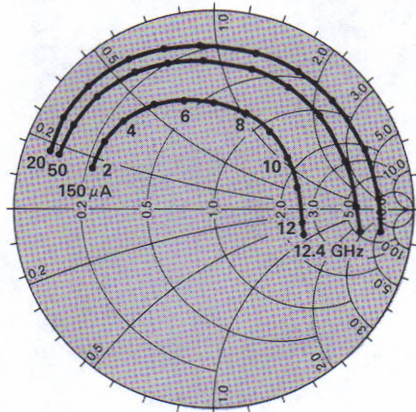


Figure 10. Typical Admittance Characteristics, 5082-2751 with external bias.

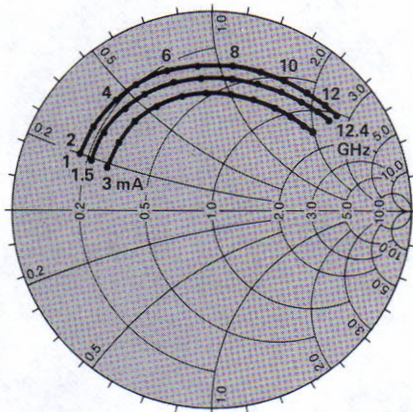


Figure 11. Typical Admittance Characteristics, 5082-2750 with self bias.

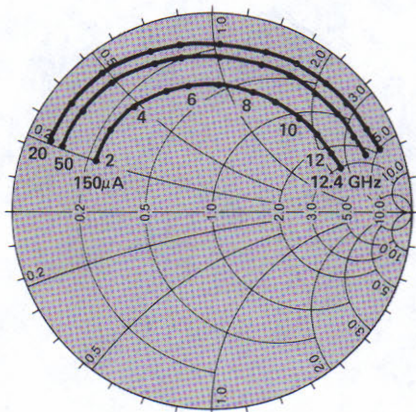


Figure 12. Typical Admittance Characteristics, 5082-2750 with external bias.

Applications for Schottky Barrier Diodes

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Broadband Microstrip Mixer Design: The Butterfly Mixer 119

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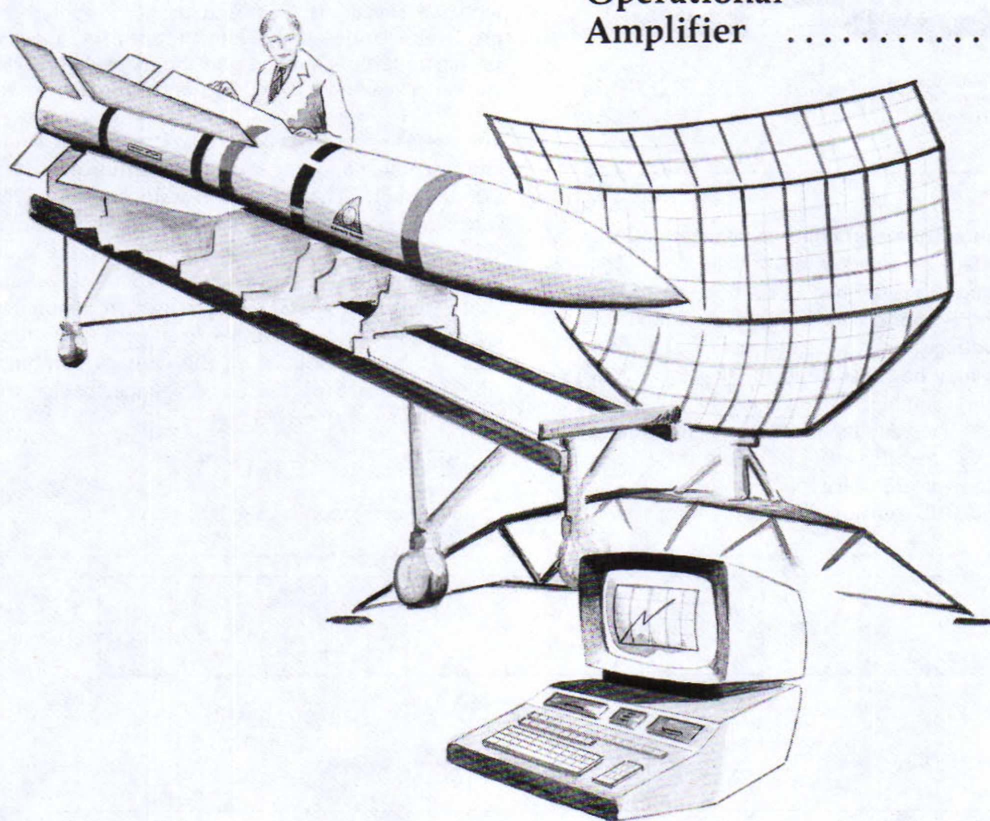
Using the HSCH-1001 Schottky Diode for Interfacing in Micro-processor Controlled A/D Conversion Circuits ... 122

Optocoupler Speed-Up Using the HSCH-1001 Schottky Diode 123

Using the 5082-2835 Schottky Diode for Protecting and Improving the Performance of an Operational Amplifier 123



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COMPONENTS

APPLICATIONS FOR SCHOTTKY DIODES

The Criterion for the Tangential Sensitivity Measurement

(Application Note 956-1)

A tangential signal is defined on a CRT display as a pulse whose bottom level coincides with the top level of the noise on either side of the pulse (Figure 1). Although the corresponding signal-to-noise ratio depends on many system factors, the generally accepted ratio of 8dB at the output correlates well with the tangential appearance on the oscilloscope for practical systems.

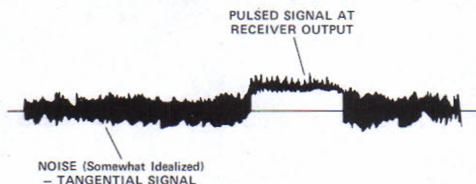


Figure 1.

The often asked question concerning whether 8dB refers to voltage or power is not a valid one. The number of decibels is defined as 10 $\log_{10}$ $(P_1 \div P_2)$ where P_1 and P_2 are power levels to be compared. If output voltages are to be compared, the ratio $(V_1 \div V_2)^2$ may be substituted for $(P_1 \div P_2)$. In this case the number of decibels is 20 $\log_{10}$ $(V_1 \div V_2)$. The number of decibels determines both $(V_1 \div V_2)$ and $(P_1 \div P_2)$. The terms "voltage dB" and "power dB" are not significant. For example, the 8dB output ratio corresponds to a power ratio of 6.3 and a voltage ratio of 2.5.

Another source of confusion is the relationship between input ratios and output ratios. Because the detector is a square law device, the output voltage is proportional to the square of the input voltage, or to the input power. A signal-to-noise voltage ratio of 2.5 at the output thus corresponds to an input power ratio of 2.5. Since 10 log 2.5 = 4, the equivalent input signal-to-noise ratio for tangential sensitivity is 4dB.

A useful production test system (Figure 2) uses an RMS voltmeter to compare signal output to noise output. The noise level is observed on the meter with RF signal off, but with d.c. bias applied to the Device Under Test. Then the specified tangential signal level is applied and the increase in RMS voltmeter reading must correspond to 8dB or more.

The use of square wave modulation and AC coupling introduce another source of confusion to this measurement. The increase in reading on the RMS voltmeter corresponding to the 8dB criterion is 4.1dB. The 8dB criterion means that the peak signal voltage is 2.5 times the RMS noise voltage V_m. Because the RMS meter uses AC coupling, the square wave is symmetrical with amplitude 1.25 V_m. The square of this voltage combines with the square of the noise voltage to give the total voltage on the RMS meter.

$$V_T^2 = V_N^2 + (1.25\ V_N)^2 = 2.56\ V_N^2$$

This ratio corresponds to 4.1dB.

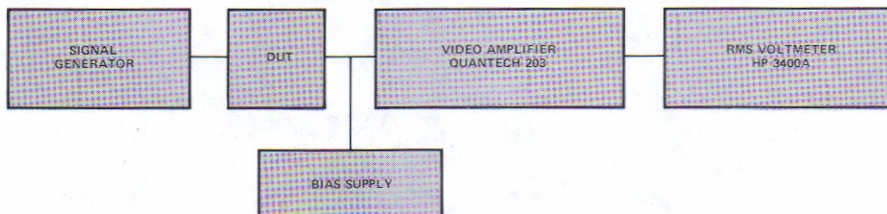


Figure 2. TSS Test System.

Broadband Microstrip Mixer Design: the Butterfly Mixer

(Portion of Application Note 976)

INTRODUCTION

In Hewlett-Packard Application Note 963, Impedance Matching Techniques for Mixers and Detectors, a technique for designing broadband matching circuits was developed and illustrated with circuits for matching the 5082-2709 beam-lead Schottky diode. The shunt elements in these circuits are shorted transmission lines with low characteristic impedance — as low as 8 ohms. No attempt was made to realize these circuits.

This Note concerns the application of this matching technique to the design and construction of a microstrip mixer using a 5082-2207 diode for the frequency range from 8 GHz to 12 GHz. The problem of realizing low impedance shunt lines was solved by using radial lines.

MATCHING PROCEDURE

Figure 1 shows the diode admittance. There are three steps in the matching procedure. First, a high impedance line transforms the admittance so that the conductance at 8 GHz equals the conductance at 12 GHz. This is shown in Figure 2. Then a shunt susceptance is added to resonate at the band edges.

For a shorted line, the correct values of characteristic impedance and length can be found by solving the equations for required susceptance at the two frequencies. The solution is 13 ohms and 91.6° at 10 GHz.

Low impedance lines are difficult to realize. The width is a significant fraction of a wavelength, so the location of the line is not well defined. By using two shunt lines, the circuit can be realized with 26 ohms lines, but this is still a very low impedance.

The use of radial lines solves this problem. Before explaining the radial line design, the rest of the matching procedure will be shown. Figure 3 shows the admittance after the shunt susceptance is added.

The final matching element is a quarter wave transformer which centers the circle on the Smith Chart. The characteristic impedance is determined by assuming that the transformer inverts the circle without changing the diameter so that the normalized admittance at 10 GHz will be changed by the transformer from 2.8 to 0.64. The required transformer impedance is $50/\sqrt{0.64 \times 2.8} = 37$ ohms. Figure 4 shows the admittance of the final circuit.

RADIAL LINE STUBS

Problems of location and parasitics of low impedance shunt stubs were solved by using fan-shaped open stubs with the narrow end connected to the main transmission line. Figure 5 shows the pertinent dimensions.

A fan-shaped stub can be considered as a portion of a radial transmission line. Assume that the reactance varies inversely as the angle so that

$$X = \frac{dZ_0}{2\pi R_i} \frac{\cos(\theta_i - \psi_L)}{\sin(\psi_i - \psi_L)} \frac{360}{\alpha}$$

where d is dielectric thickness and

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_r}} \sqrt{\frac{J_0^2(kR_i) + N_0^2(kR_i)}{J_1^2(kR_i) + N_1^2(kR_i)}}$$

$$k = \frac{2\pi\sqrt{\epsilon_r}}{\lambda_0}$$

$$\theta = \tan^{-1}\left[\frac{N_0(kR_i)}{J_0(kR_i)}\right]$$

$$\psi_{i,L} = \tan^{-1}\left[\frac{J_1(kR_{i,L})}{-N_1(kR_{i,L})}\right]$$

There is a question about the use of ϵ_r, dielectric constant of the medium, in these equations. When α is close to 360°, it appears logical to use ϵ_r because the circuit is close to a radial line where ϵ_r is correct. However, when the angle is small, the stub is very close to a microstrip stub, so it seems logical to use the microstrip expression,

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 10\frac{h}{w}\right)^{-1/2}$$

where h is the dielectric thickness and w is the line width. In this analysis, the width corresponding to splitting the stub area in half is used for W.

When a stub with parallel edges is used for the shunt elements, the solution for characteristic impedance and length requires the solution of two simple equations for the required reactances at band edge frequencies. However, the radial stub equations are not simple and there are three unknowns: angle and inner and outer radii. A third equation requiring zero reactance at center frequency could be introduced, but the solution of three simultaneous equations involving four types of Bessel functions would require considerable computer capability.

The problem is simplified by assuming a reasonably small value for the inner radius such as 0.51 mm (0.020 inch) and solving for R_L from the equation for the ratio of required reactances at the band edge frequencies. From Figure 2, the ratio is $(1.16/-1.40)^{-1} = -1.21$.

Since the equation must be solved by substitution, it is convenient to plot $X\alpha$ at 8 GHz and 12 GHz as functions of R_L. This is shown in Figure 6 where it is seen that the desired ratio occurs near $R_L = 12$ mm.

Figure 7 expands the region near this value of R_L and shows a solution at $R_L = 11.68$ mm. Dividing $X\alpha$ at either 8 GHz or 12 GHz by the known value of X gives $\alpha = 206°$. It is not possible to have an angle greater than 180°, but this problem is solved by using two shunt stubs. This requires double the reactance for each stub, so $\alpha = 103°$ C.

Note that the slope of reactance at 12 GHz, with respect to R_L, is steep, while the slope at 8 GHz is shallow. This behavior is confirmed in the experimental mixer. Changes in R_L have little effect on the impedance at 8 GHz, while the impedance at 12 GHz is quite sensitive.

The substrate material is RT/duroid 5880 with a dielectric constant of 2.2. The effective dielectric constant, ϵ_{eff}, for the half area width is 2.10.

EXPERIMENTAL CIRCUIT

Figure 8 shows the circuit built to demonstrate this design procedure. Noise figure at 9.375 GHz is 6.7 dB compared to 6.0 dB for the diode in the narrow band production test fixture.

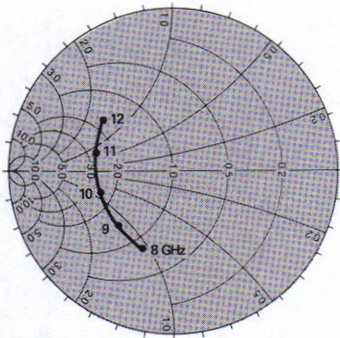
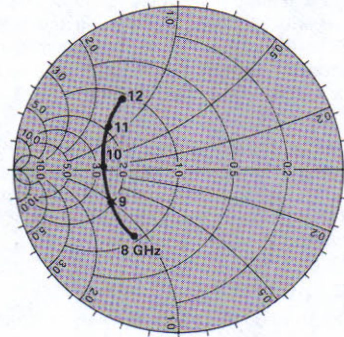


Figure 1. Diode Admittance.



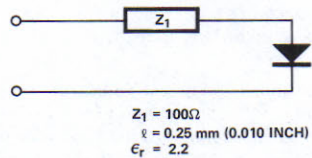
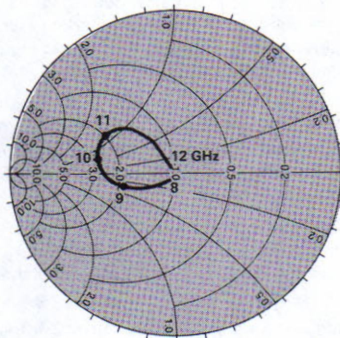


Figure 2. Admittance of Diode with High Impedance Line.



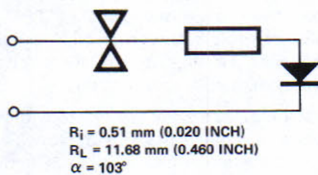
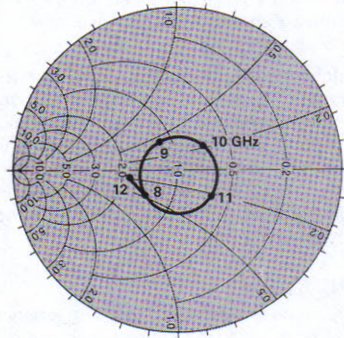


Figure 3. Admittance of Resonated Mixer Circuit.



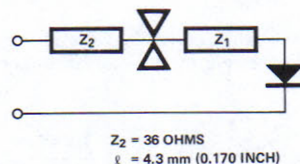


Figure 4. Computed Mixer Admittance.

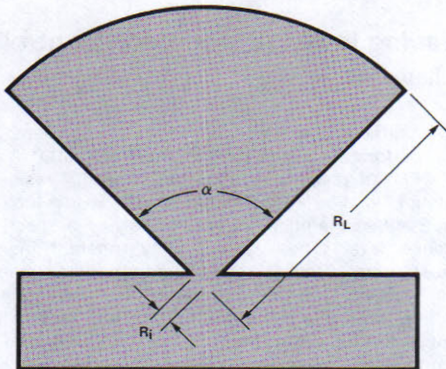


Figure 5. Radial Stub.

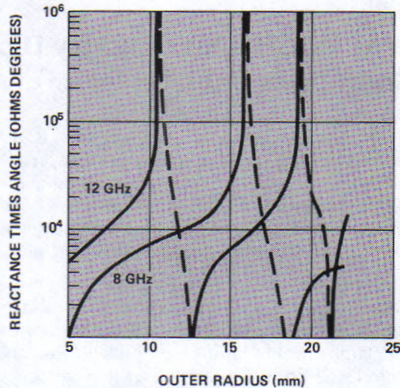


Figure 6. Radial Stub.

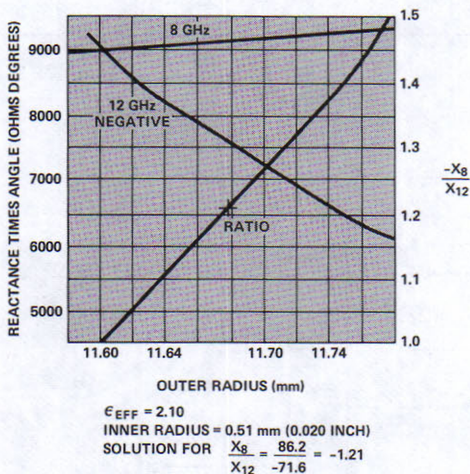


Figure 7. Radial Line Analysis.

Figure 8. Photograph of the Butterfly Mixer.

Transistor Speed Up Using Schottky Diodes (Portion of Application Bulletin 13)

NONSATURATING TRANSISTOR SWITCHES

The operation of a transistor switching circuit in the saturation region produces fast turn-on times, but slow turn-off times as a result of storage delay. Excess base current needed to drive the transistor into saturation causes an accumulation of stored charge in the base region, which must be removed before the transistor switch can turn off. Various schemes have been devised to overcome the storage delay and speed up switching time by not allowing the transistor to saturate and minimizing turn-off delay.

A very effective way of preventing saturation, using Hewlett-Packard diodes, is illustrated in the circuit in Figure 1.

Significant reduction in transistor switching delay time can be achieved by adding a Schottky diode (5082-2811), (or HSCH-1001) and a PIN diode (5082-3077) to the transistor switch.

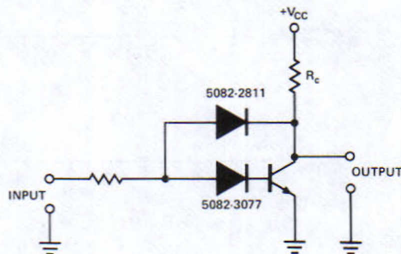


Figure 1. The Use of Diodes as Feedback Elements to Avoid Saturation in a Transistor Switch.

Using the HSCH-1001 Schottky Diode for Interfacing in Microprocessor Controlled A/D Conversion Circuits (Portion of Application Bulletin 26)

The use of custom codec (coder/decoder) IC chips simplifies the analog to digital circuitry in microprocessor controlled digital switching circuits. For optimum circuit performance, the required compatible interface between the codec chip and the rest of the circuit can be achieved with the help of HSCH-1001 (IN6263) Schottky diodes.

Details of the analog to codec chip interfacing circuitry are shown in Figure 1. TTL D-type flip-flops are used in the modulator and demodulator. The four Schottky diodes act as voltage clamps for the flip-flop outputs. Proper choice of these diodes is critical in achieving the performance characteristics desired.

Diode characteristics required for optimum clamping circuit performance are found in the HSCH-1001. Very high OFF/ON resistance ratios of 10^7 to 10^8 result in maximum isolation and minimum loss. The low turn on voltage allows clamping more precisely to a specified reference level. The reproducibility inherent in the manufacturing process gives uniform performance characteristics. The reverse breakdown voltage and switching speed of the HSCH-1001 are more than adequate for this application. The HSCH-1001 would be useful for high speed digital applications in excess of 1 Gigabit/sec and at voltage levels as high as 60 volts.

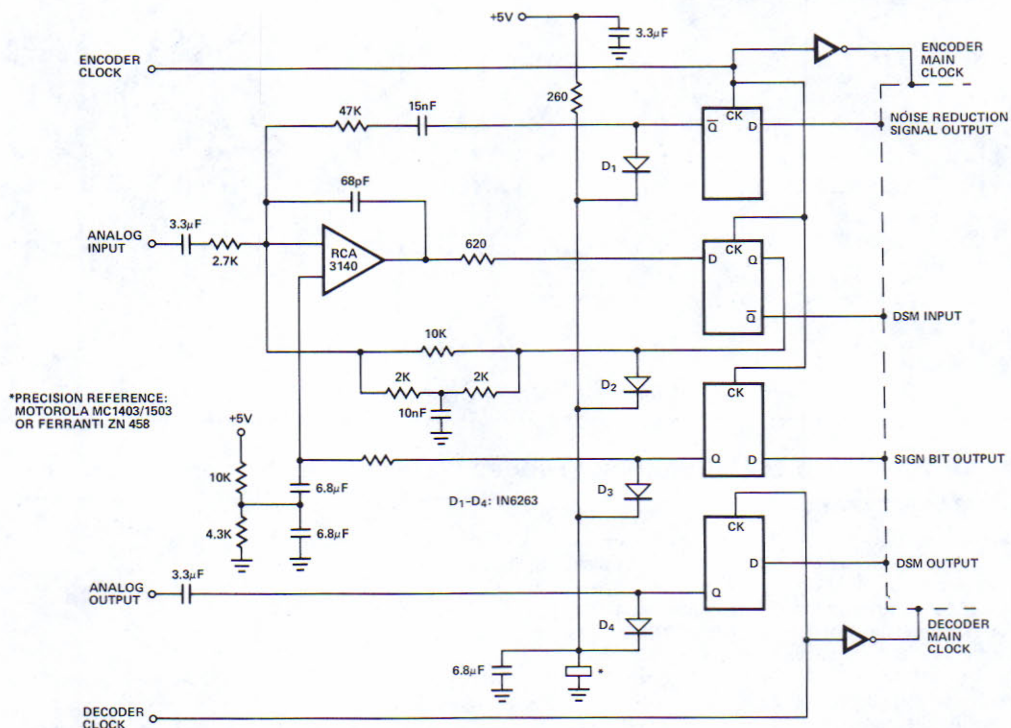


Figure 1. Details of the Analog to Codec Chip Interfacing Circuitry.

Optocoupler Speed-Up Using the HSCH-1001 Schottky Diode
(Portion of Application Bulletin 28)

An optocoupler typically contains a bipolar transistor in the output circuit. When a positive input signal is applied, a saturated turn-on of the transistor results, which means that the turn-off time will be unnecessarily long. The HSCH-1001 Schottky diode can be used to alleviate the saturation effects on the transistor and thus improve switching time.

CIRCUIT PERFORMANCE

Shown in Figure 1 is the switching test circuit for the 6N139 optocoupler together with the input and output waveforms. The HSCH-1001 is placed in parallel with the base-collector junction (pins 7 and 6) of the output transistor. The HSCH-1001 has a lower turn-on voltage than a P-N junction, so when the transistor is driven into saturation, the HSCH-1001 bypasses the current which would otherwise enter the base-collector junction. With reduced current entering the base-collector junction, there is a proportionate reduction in the charge to be removed when the transistor is to be turned off. Thus, the HSCH-1001 acts as a clamp to reduce the turn-off delay.

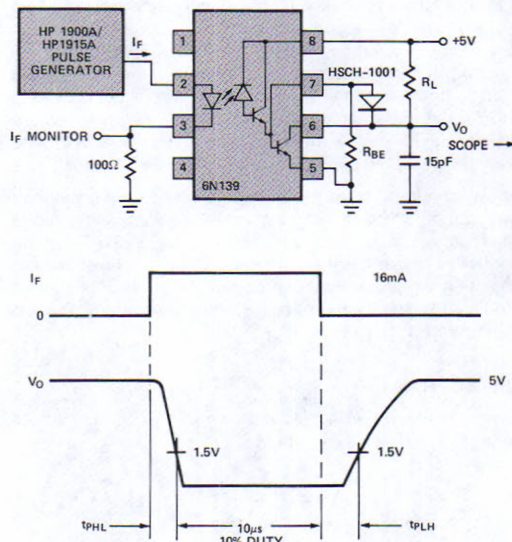


Figure 1. The 6N139 Optocoupler Switching Test Circuit with Input and Output Waveforms.

Using the 5082-2835 Schottky Diode for Protecting and Improving the Performance of an Operational Amplifier (Portion of Application Bulletin 30)

High level voltage spikes degrade the performance of an operational amplifier. In extreme cases the operational amplifier is destroyed permanently. The use of 5082-2835 Schottky diodes for clamping the input signal to an operational amplifier not only provides protection against high level voltage overload, but also improves output response.

Protection of an operational amplifier from high input voltages can be achieved by using a two-diode (5082-2835) clamp as shown in Figure 1. The diodes limit the voltages at the input to the operational amplifier to safe levels.

In addition to providing protection, the Schottky clamp in Figure 1 will suppress spurious output and reduce settling time for an operational amplifier. Settling time is the total time needed for the output to slew through a specified voltage change and settle to the final voltage within a prescribed percentage error.

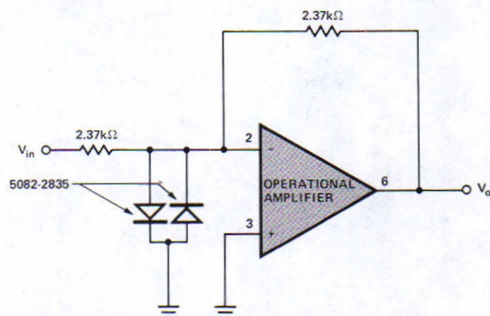


Figure 1. A Two-Diode (5082-2835) Clamp Provides Protection for an Operational Amplifier from High Input Voltages and also improves output response.

Square Law and Linear Detection (Portion of Application Note 986)

INTRODUCTION

Schottky diode detectors are used to detect small signals close to the noise level and to monitor large signals well above the noise. From the noise level up to about -20 dBm (Figure 1) the slope of the response curves is constant. This is the square law region. Video receivers usually operate in this range. The diode receives the signal directly from the antenna in most systems, although a preamplifier may be used to improve sensitivity. This type of receiver is used in short range radar or in counter-measure equipment where the sensitivity of the more complicated superheterodyne receiver is not needed.

Above about -10 dBm the slope is closer to linear but may vary about 30% for different values of frequency, diode capacitance, and load resistance. The slope may be controlled by tuning at the proper power level. Linear detection is used in power monitors. In some applications the linearity is important because the detected voltage is a measure of power input.

DETECTION LAW

Over a wide range of input power level, P, the output voltage, V, follows the formula

$$V = K(\sqrt{P})^{\alpha}$$

At low levels, below -20 dBm, α is two. This is the square law region. When DC bias current is used (usually microamperes), the diode impedance is independent of power level so the tuning can be done at any level. Usually the diode is tuned at -30 dBm. The detected voltage at this level is called the voltage sensitivity.

At higher power levels the diode impedance changes with power. At these levels, the value of α can be as low as 0.8 (Figure 2). The slope is related to diode capacitance, frequency, and load resistance. When the circuit is retuned at each power level, the output and the slope increase.

FREQUENCY AND DIODE CAPACITANCE — EFFECT ON VOLTAGE SENSITIVITY

The diode junction capacitance shunts the junction resistance. Detected voltage is reduced because some of the input current flows through the capacitance and never reaches the resistance where detection takes place. The effect is more serious at higher frequencies because capacitance susceptance is proportional to frequency. Similarly, the effect is more serious for higher capacitance diodes.

FREQUENCY AND DIODE CAPACITANCE — EFFECT ON SLOPE IN HIGH LEVEL DETECTION

Figure 3 shows how the slope of the detection characteristic becomes steeper at higher frequencies. The output voltage at 2 GHz is nearly equal to the 1 GHz voltage above 22 dBm. The main reason for this behavior is the lower value of junction resistance at higher power. This is explained in greater detail in the Appendix.

Since frequency and diode capacitance appear in the degradation factor as the product fC, the increasing slope at higher frequency also happens at higher capacitance. This is shown in Figure 4 where the detection characteristic for the higher capacitance 5082-2800 diode is steeper than the characteristic for the -2824 diode.

EFFECT OF BREAKDOWN VOLTAGE

In Figure 4 the curves cross so that above 22 dBm the voltage detected by the -2800 is higher than the voltage detected by the lower capacitance -2824 diode. The degradation factor analysis does not explain this crossover. It is related to the effect of breakdown voltage. At high power levels the negative portion of the input signal is large enough to cause reverse conduction. This negative detected voltage reduces the output level and the curve levels off. At higher levels the negative detected voltage will predominate and the curve will reverse direction and have a negative slope.

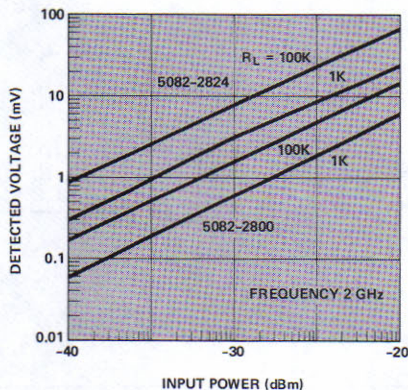


Figure 1. Square Law Response.

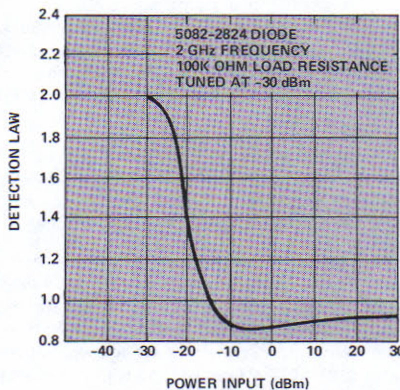


Figure 2. Variation of Detection Law with Input Power.

The -2800 diode has a high voltage breakdown and so does not exhibit this reverse conduction effect.

TUNING FOR LINEAR RESPONSE

In applications where the detector is used as a power meter linear detector response is needed. Microprocessors are often available to correct the diode response but this involves added expense. Reducing the load resistance can often produce the desired response but the sensitivity is reduced. Figure 5 shows how the sensitivity can be improved while the response is corrected. When the slope is too shallow (the usual case) the correction can be made by tuning at a higher level instead of tuning at -30 dBm. In this case the tuning level was +20 dBm. If the circuit is tuned for maximum output at 20 dBm the response will be too steep. A few iterations are necessary to get the response shown.

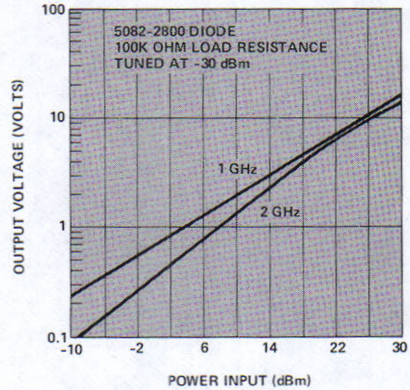


Figure 3. Higher Frequency Increases Slope.

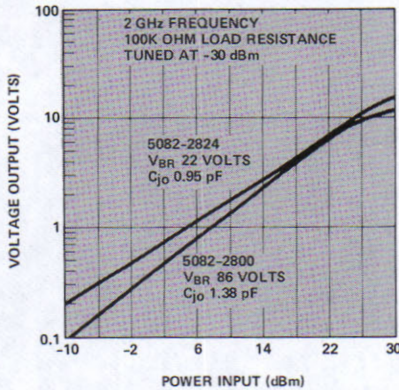


Figure 4. Higher Capacitance Increases Slope.

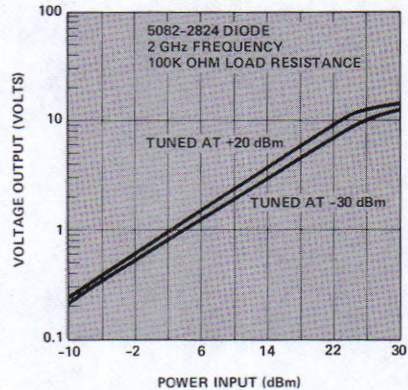


Figure 5. Tuning for Linear Response.

PIN Diodes & High Conductance Diodes

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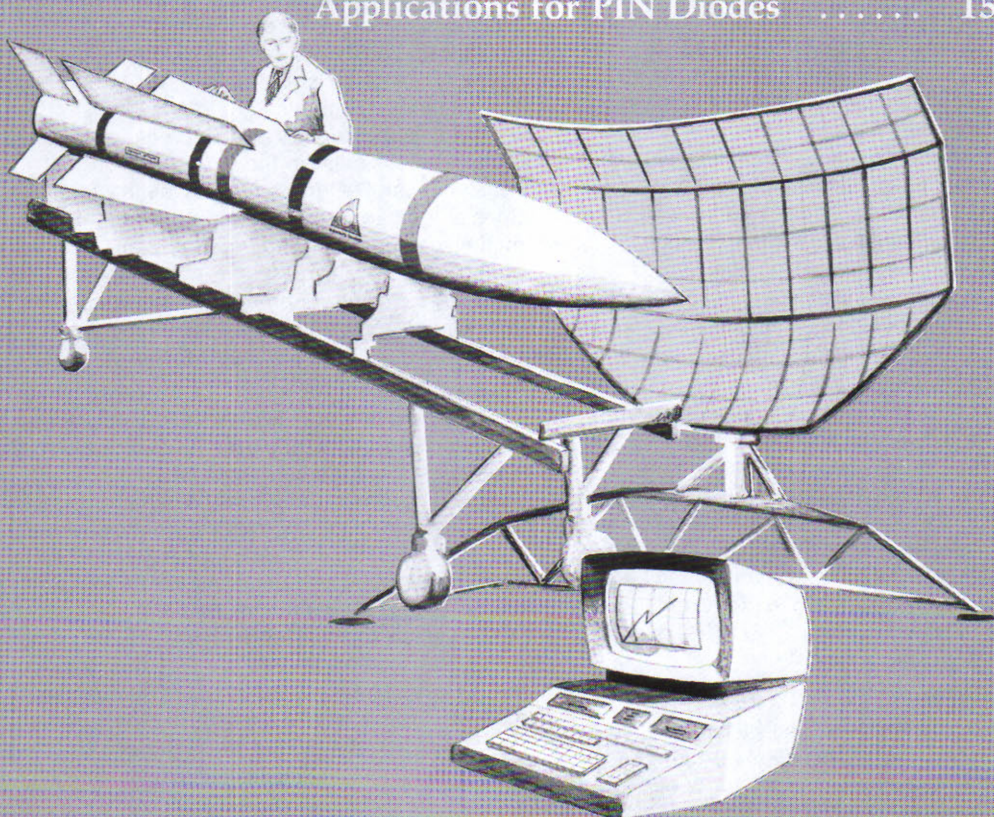


The PIN Diode

The most important feature of the PIN diode is its basic property of being an almost pure resistor at RF frequencies, whose resistance value can be varied from approximately 10,000 ohms to less than 1 ohm by the control current flowing through it. Most diodes exhibit this characteristic to some degree, but the PIN diode is typically optimized in design to achieve a relatively wide resistance range, good linearity, low distortion, and low current drive. The characteristics of the PIN diode make it suitable for use in switches, attenuators, modulators, limiters, phase shifters, and other signal control circuits.

Device Characteristics

The principal parameters of a PIN diode which play major roles in determining the performance of a circuit include the following:

RF Resistance

The PIN diode structure consists of an I (Intrinsic) layer of very high resistivity material sandwiched between regions of highly doped P (positively charged) material and N (negatively charged) material. With reverse or zero bias, the I-layer is depleted of charges and the PIN diode exhibits very high resistance. When forward bias is applied across the PIN diode, positive charge from the P region and negative charge from the N region are injected into the I-layer, therefore increasing its conductivity and lowering its resistance. The high off resistance and low on resistance make the PIN diode attractive for switching applications.

At RF frequencies, the PIN diode with forward bias behaves essentially as a pure resistor. The resistance of the PIN diode is related to the bias current, the geometry of the I-layer and the properties of the carriers. For a given type of PIN diode with uniform characteristics, resistance is inversely proportional to the forward bias current. Whereas, only high off resistance and low on resistance are important in switching applications, the resistance characteristics in the entire dynamic range are of concern in attenuator applications. Linearity of resistance with bias makes the PIN diode useful for attenuator applications.

Carrier Lifetime

An important parameter of the PIN diode is the carrier lifetime, τ, which is useful for defining the low frequency limit, $f_o = \frac{1}{2\pi\tau}$, for linear performance of the diode. For RF signal frequencies below fo, the PIN diode rectifies the signal much like an ordinary PN junction diode, and considerable output distortion results. (See Application Note 957-3 for additional discussion on rectification causes and effects). At frequencies above fo, less rectification occurs with increasing frequency, allowing the PIN diode to appear more linear, approaching a pure resistor.

For applications requiring good linearity and low distortion the minimum signal frequency should be ten times fo, i.e., $f_{min} = \frac{10}{2\pi\tau}, = \frac{1.6}{\tau}$. This restriction is not important in switching applications, where the diode is normally biased either completely off or on. In those states, since most of the power is either reflected or transmitted, the effect of RF current on the total charge is small and distortion is not a problem.

Capacitance

Diode capacitance limits switch and attenuator performance at high frequencies in the form of isolation rolloff and increased insertion loss. Optimum performance can be achieved by one of several alternatives available. Using a low capacitance diode would be one solution. Since the junction capacitance of a PIN diode is related to the geometry and electrical properties of the I-layer similar to the case of RF resistance, an R-C trade-off may be feasible. Special techniques can be employed to minimize capacitive (and other parasitic) effects, and in some cases even to take advantage of them. (Some of the techniques for improving high frequency performance are discussed in Application Notes 922 and 957-2.)

Reverse Recovery Time

Reverse recovery time is a measure of switching time, and is dependent on the forward and reverse bias applied. With forward bias current, charge is stored in the I-layer. When a reverse pulse is applied, reverse current will flow for a short period of time, known as delay time, t_d. When a sufficient number of carriers have been removed, the current begins to decrease. The time required for the reverse current to decrease from 90% to 10% is called the transition time, t_t. The sum, $t_d + t_t$, is the reverse recovery time, which is a measure of time it takes to switch the diode from on to off.

Reverse Breakdown Voltage

The reverse breakdown voltage defines the recommended maximum signal level for safe operation of the diode. Operation at signal levels above the reverse breakdown voltage may result in degradation of diode characteristics or in permanent damage to the diode.

Circuit Performance

The performance of a PIN diode circuit is directly related to the basic characteristics of the diode. As an illustrative example, the performance of a PIN diode switch can be simply approximated by treating the PIN diode essentially as a resistor in the forward biased state and a capacitor in the reverse biased state. Switch performance can then be analyzed as follows:

Insertion Loss

The loss of signal attributed to the diode when the switch is on (transmission state) is insertion loss. For low insertion loss, low resistance is needed in a series switch (Figure 1). Low capacitance (particularly at high frequencies) is needed in a shunt switch.

Isolation

Isolation is the measure of RF leakage between the input and output when the switch is off. For high isolation (low transmission) low capacitance is required in a series switch especially at high frequencies (Figure 2). Low resistance is required in a shunt switch.

Switching Speed

As discussed before, reverse recovery time is a measure of switching time.

Power Handling Capability

The RF power (CW or pulse) that can be handled safely by a diode switch is limited by two factors — the breakdown voltage of the diode, and thermal considerations, which involve the maximum junction temperature and the thermal resistance of the diode and packaging. Other factors affecting power handling capability are ambient temperatures, frequency, attenuation level (which is related to diode resistance), pulse width and duty cycle. A first order approximation of the power handling capability of the PIN diode can be obtained by using the procedure entitled "Power Handling Capability of PIN Diode Switches and Attenuators" discussed in the section on Applications for PIN Diodes. A similar performance analysis as the above can be extended to attenuator, limiter and other applications.

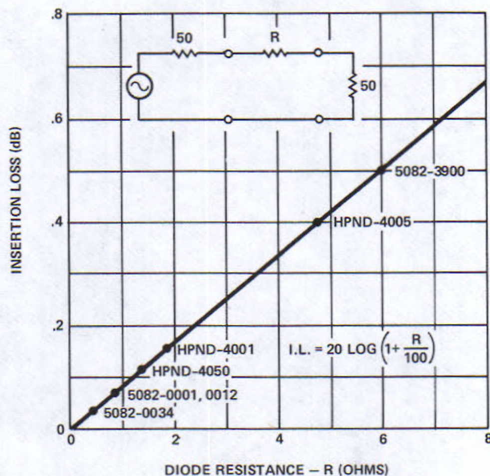


Figure 1. Insertion Loss of Series Diode Switch

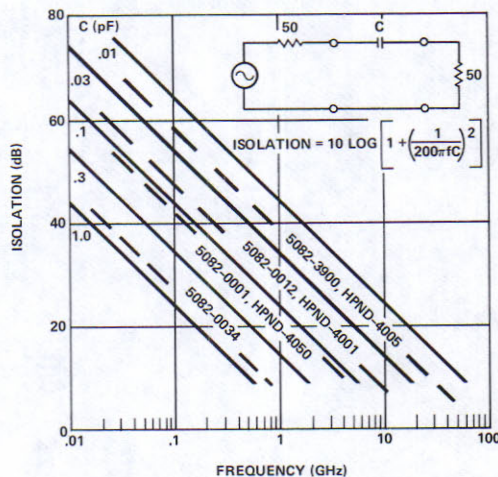


Figure 2. Isolation of Series Diode Switch

PIN Diodes

Diode Selection

Hewlett-Packard PIN diodes are available in chip form and several types of packages, which lend themselves more suitable for particular applications. Packaged devices containing the generic chips are listed in the Selection Guide in the order of increasing junction capacitance.

For switching, attenuating, and other general purpose applications particularly in the VHF/UHF range, the low cost glass package (Outline 15) is suitable. Due to their low parasitics, ceramic packages (Outlines 31 and 38) are suited for broadband circuits up to 1 GHz and for resonated narrowband circuits up to 8 GHz. In addition, they have medium power handling capability.

Stripline packages (Outlines 60 and 61), containing built-in low pass matching circuits, can be used in broadband designs up to 18 GHz. Because of good heat sinking, they can handle high power in switching, attenuating and limiting applications. The beam lead packages with low parasitics are designed for use in stripline or microstrip circuits using welding or thermo-compression bonding techniques. The lid (Outline 50) and ministrip (Outlines 71, 72) packages are intended to facilitate handling and assembly for use in hybrid integrated circuits.

PIN Diodes Selection Guide

(Devices listed in the order of increasing junction capacitance)
All part numbers, 5082- (except HPND- as noted)

Maximum Junction Capacitance C_{JVR} (pF) (Note 1)	Typical RF Resistance R_s (Ω) (Note 3)	Chip (Note 4)	Packaged Devices Containing Similar Chips (Package Outline)								
			Beam Lead (Note 4)	LID (50) (Note 4)	Mini Strip (72) (Note 4)	Post (74) (Note 4)	Glass (15)	Ceramic (31)	Ceramic (38)	Stripline (60)	Stripline (61)
0.02***	4.7††		HPND-4005								
0.025****	6.0†		3900								
0.08*	1.8†††		HPND-4001								
0.12	0.8	0012		3005	3000	3259	3001 3002 3039 3077 1N5719 HPND-4165 HPND-4166	3201 3202	3101 3102	3140	3040
0.12	0.8	0030						3303 3304		3170	3340
0.15	0.6	0047									
0.15***	1.3†††		HPND-4050								
0.16**	0.8††	0001				3258	3042 3043	3306	3305	3141	3041 3071
0.20	1.5	0025					3080 3379 1N5767				
0.20	2.0	0039					3081				
0.20	0.6	0049									3046
1.2**	0.4†††	0034					3168 3188				
Package Capacitance (pF)			(Note 2)	.18	.13	.13	.13	.2	.2	.03	.03
Pages											

Notes:

1. All capacitance measured with $V_R = 50$ volts, except:
   *$V_R = 30$ volts
   **$V_R = 20$ volts
   ***$V_R = 10$ volts
   ****$V_R = 0$ volt
2. Capacitance of beam lead devices includes package capacitance.
3. RF resistance measured with $I_F = 100$ mA, except:
   †$I_F = 50$ mA
   ††$I_F = 20$ mA
   †††$I_F = 10$ mA
4. Detailed specifications are available in the Section on Devices for Hybrid Integrated Circuits.

HEWLETT PACKARD

PIN DIODES FOR RF SWITCHING AND ATTENUATING

1N5719 *
1N5767 *
5082-3001/02
5082-3039 *
5082-3042/43
5082-3077 *
5082-3080 *
5082-3081
5082-3168/88 *
5082-3379
HPND-4165/66

Features

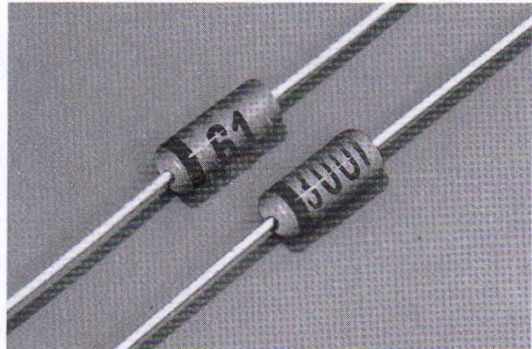
LOW HARMONIC DISTORTION

LARGE DYNAMIC RANGE

LOW SERIES RESISTANCE

LOW CAPACITANCE

LOW TEMPERATURE COEFFICIENT
Typically Less Than 20% Resistance Change from 25°C to 100°C



Description / Applications

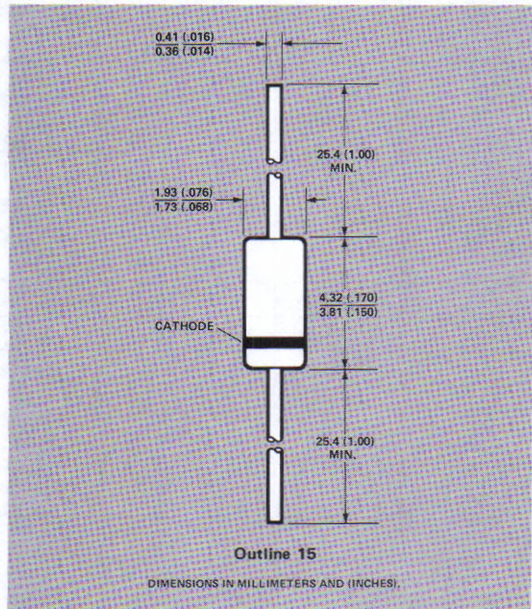
These general purpose switching diodes are intended for low power switching applications such as RF duplexers, antenna switching matrices, digital phase shifters, and time multiplex filters. The 5082-3168/3188 are optimized for VHF/UHF bandswitching.

The RF resistance of a PIN diode is a function of the current flowing in the diode. These current controlled resistors are specified for use in control applications such as variable RF attenuators, automatic gain control circuits, RF modulators, electrically tuned filters, analog phase shifters, and RF limiters.

Mechanical Specifications

The HP Outline 15 package has a glass hermetic seal with dumet leads. The lead finish is tin for all PIN diode products except the 5082-3042 and -3043, which have gold plated leads. The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch (1.6mm) from the glass body. With this restriction, Outline 15 package will meet MIL-STD-750, Method 2036, Conditions A (4 lbs., [1.8 kg.], tension for 30 minutes) and E. The maximum soldering temperature is 230° C for five seconds. Typical package inductance and capacitance are 2.5 nH and 0.13pF, respectively. Marking is by digital coding with a cathode band.

Package Dimensions



Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

Power Dissipation 250mW
(Derate linearly to zero at 150°C)

Peak Inverse Voltage (PIV) .... V_{BR}

*Also available in Tape and Reel.
Please contact local HP Sales Office for further information.

General Purpose Diodes

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Maximum Total Capacitance C_T (pF)	Minimum Breakdown Voltage V_{BR} (V)	Maximum Residual Series Resistance R_S (Ω)	Minimum Effective Carrier Lifetime τ (ns)	Maximum Reverse Recovery Time t_{rr} (ns)
GENERAL PURPOSE SWITCHING AND ATTENUATING					
3002	0.2	300	1.0	100	100 (typ)
3001	0.25	200	1.0	100	100 (typ)
3039	0.25	150	1.25	100	100 (typ)
IN5719	0.3**	150	1.25	100	100 (typ)
3077	0.3	200	1.5	100	100 (typ)
FAST SWITCHING					
3042	0.4*	70	1.0*	15 (typ)	5
3043	0.4*	50	1.5*	15 (typ)	10
BAND SWITCHING					
3188	1.0*	35	0.6**	40 (typ)	12 (typ)
3168	2.0*	35	0.5**	40 (typ)	12 (typ)
Test Conditions	V_R = 50V *V_R = 20V **V_R = 100V f = 1 MHz	$V_R = V_{BR}$ Measure $I_R \leqslant 10\mu A$	I_F = 100mA *I_F = 20mA **I_F = 10mA f = 100 MHz	I_F = 50mA I_R = 250mA	I_F = 20mA V_R = 10V 90% Recovery

Note: Typical CW power switching capability for a shunt switch in a 50Ω system is 2.5W.

RF Current Controlled Resistor Diodes

Electrical Specifications at $T_A = 25°C$

Part Number	Minimum Effective Carrier Lifetime τ	Minimum Breakdown Voltage V_{BR}	Maximum Residual Series Resistance R_S	Maximum Total Capacitance C_T	High Resistance Limit, R_H		Low Resistance Limit, R_L		Maximum Difference in Resistance vs. Bias Slope, Δx
					Min.	Max.	Min.	Max.	
HPND-4165	100	100	1.5	0.3	1100	1660	16	24	.04
HPND-4166	100	100	1.5	0.3	830	1250	12	18	.04
5082–3080*	1300(typ)	100	2.5	0.4	1000			8**	
5082–3379	1300(typ)	50		0.4				8**	–
5082–3081	2000(typ)	100	3.5	0.4	1500			8**	
Units	ns	V	Ω	pF	Ω		Ω		–
Test Conditions	I_F=50mA I_R=250mA	$V_R=V_{BR}$, Measure $I_R \leqslant 10\mu A$	I_F=100mA f=100mHz	V_R=50V f=1mHz	I_F=0.01mA f=100mHz		I_F=1.0mA **I_F=20mA f=100mHz		Batch Matched at I_F=0.01mA and 1.0mA f=100mHz

*The 1N5767 has the additional specifications: τ = 1.0 μsec minimum
I_R = 1 μA maximum at V_R = 50V
V_F = 1V maximum at I_F = 100mA.

Typical Parameters

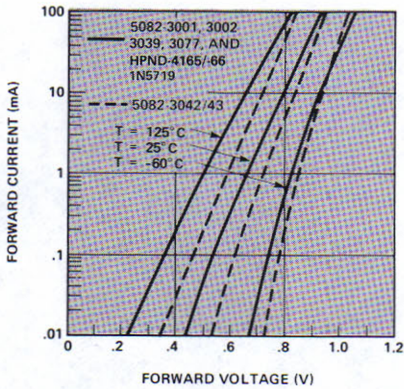


Figure 1. Typical Forward Current vs. Forward Voltage.

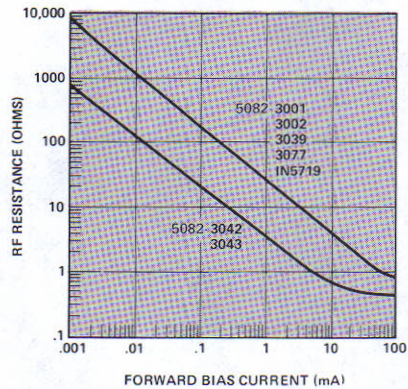


Figure 2. Typical RF Resistance vs. Forward Bias Current.

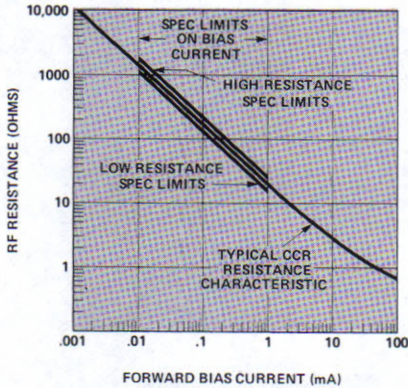


Figure 3. Typical RF Resistance vs. Bias for HPND-4165.

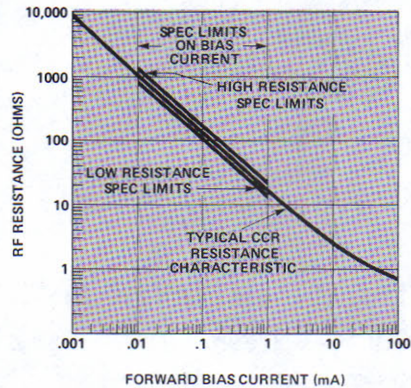


Figure 4. Typical RF Resistance vs. Bias for HPND-4166.

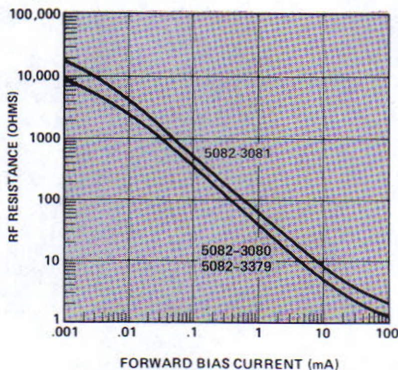


Figure 5. Typical RF Resistance vs. Forward Bias Current.

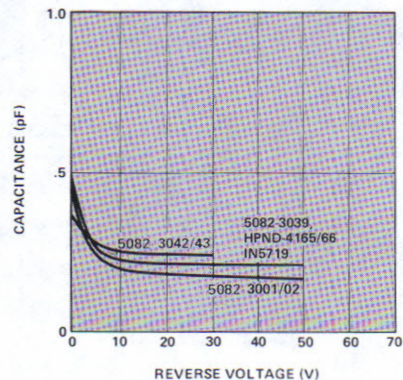


Figure 6. Typical Capacitance vs. Reverse Voltage.

Typical Parameters (Continued)

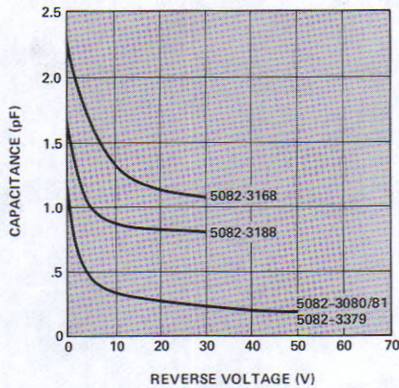


Figure 7. Typical Capacitance vs. Reverse Voltage.

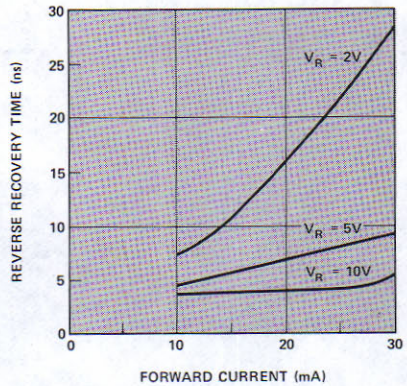


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3042, 3043.

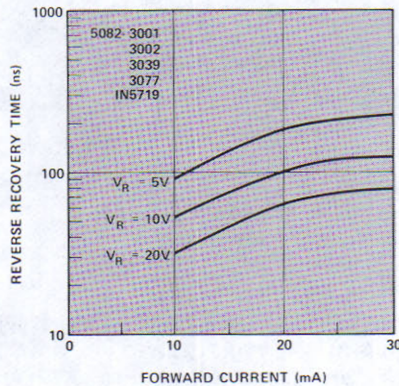


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages.

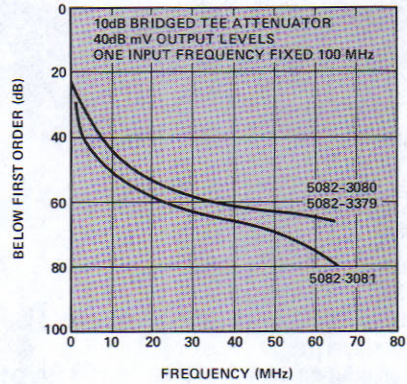


Figure 10. Typical Second Order Intermodulation Distortion.

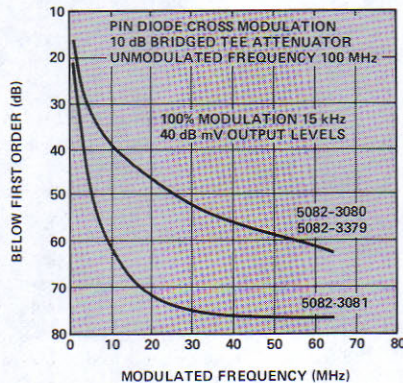


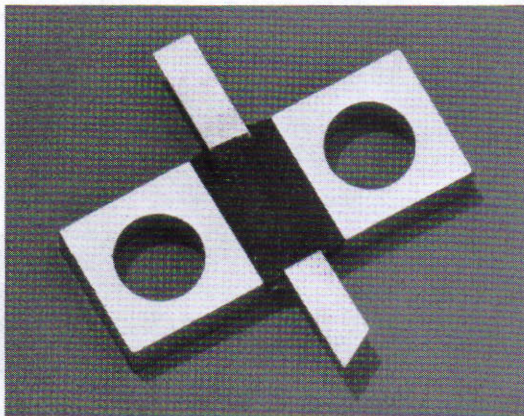
Figure 11. Typical Cross Modulation Distortion.

PIN Diodes

HEWLETT PACKARD

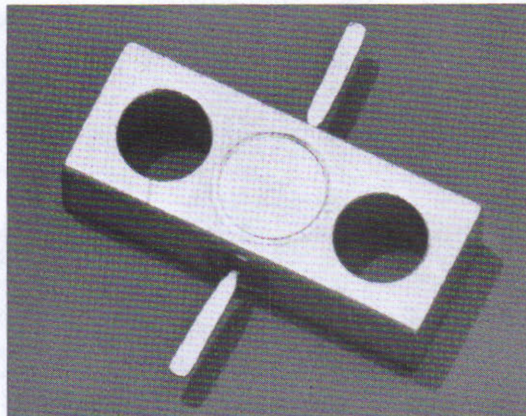
PIN DIODES FOR STRIPLINE AND MICROSTRIP SWITCHES ATTENUATORS AND LIMITERS

5082-3040/41
5082-3046
5082-3071
5082-3140/41
5082-3170
5082-3340



Features

- **HERMETIC**
  (5082-3140, 3141, 3170)
- **BROADBAND OPERATION**
  HF through X-band
- **LOW INSERTION LOSS**
  Less than 0.5 dB to 10 GHz (5082-3140, 3170)
- **HIGH ISOLATION**
  Greater than 20 dB to 10 GHz (5082-3140, 3170)
- **FAST SWITCHING/MODULATING**
  5 ns typical (5082-3141)
- **LESS DRIVE CURRENT REQUIRED**
  Less than 20 mA for 20 dB isolation (5082-3141)



Features

- **LOW COST TO USE**
  Designed for easy mounting
- **BROADBAND OPERATION**
  HF through Ku-band
- **LOW INSERTION LOSS**
  Less than 0.5 dB to 10 GHz (5082-3040, 3340)
- **LOW DRIVE CURRENT REQUIRED**
  Less than 20 mA for 20 dB isolation (5082-3041)
- **FAST SWITCHING MODULATION**
  5 ns typical (5082-3041)
- **HIGH POWER LIMITING**
  50 W peak pulse power (5082-3071)

Description

When forward biased these PIN diodes will appear as current variable resistors in shunt with a 50 ohm transmission line. The resistance varies between less than 1 ohm at high forward bias to greater than 10,000 ohms at zero or reverse bias.

The HP 5082-3040, -3046, -3340, -3140 and -3170 are passivated planar devices. The HP 5082-3041, -3071 and -3141 are passivated mesa devices. All of the devices are in a shunt configuration in stripline packages. These diodes are optimized for good continuity of characteristic impedance which allows a continuous transition when used in 50 ohm microstrip or stripline circuits.

Of these devices, the HP 5082-3040, -3041, -3046, -3071 and -3340 are in HP Package Outline 61.

The HP 5082-3140, -3141 and -3170 are in HP Package Outline 60. This package is hermetic and can be used for Hi-Rel applications. The HP 5082-3140, -3141 and -3170 are direct mechanical replacements for Outline 61 (with top cap in place) diodes HP 5082-3040, -3041, and -3340 respectively. The only electrical difference is the location of the chip in each package. Except in those few applications where the difference in phase relationship is important, the Outline 60 devices can be used as replacements.

The HP 5082-3071 passive limiter chip is functionally integrated into a 50 ohm transmission line to provide a broadband, linear, low insertion loss transfer characteristic for small signal levels. At higher signal levels self-rectification reduces the diode resistance to provide limiting as shown in Figure 6. Limiter performance is practically independent of temperature over the rated temperature range.

Applications

SWITCHES/ATTENUATORS

These diodes are designed for applications in microwave and HF-UHF systems using stripline or microstrip transmission line techniques.

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band.

These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3340 and 5082-3170 are reverse polarity devices with characteristics similar to the 5082-3040 and 5082-3140 respectively.

The 5082-3041 and 5082-3141 are recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for maximum attenuation is required.

The 5082-3046 has been developed for high peak pulse power handling as required in TR switches for distance measurement and TACAN equipment. The long effective minority carrier lifetime provides for low intermodulation products down to 10 MHz.

More information is available in HP Application Note 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

LIMITER

The 5082-3071 limiter module is designed for applications in telecommunication equipment, ECM receivers, distance measuring equipment, radar receivers, telemetry equipment, and transponders operating anywhere in the frequency range from 500 MHz through 10 GHz. An external dc return is required for self bias operation. This dc return is often present in the existing circuit, i.e. inductively coupled antennas, or it can be provided by a $\lambda/4$ resonant shunt transmission line. Selection of a high characteristic impedance for the shunt transmission line affords broadband operation. Another easy to realize dc return consists of a small diameter wire connected at a right angle to the electric field in a microstrip or stripline circuit. A 10 mA forward current will actuate the PIN diode as a shunt switch providing approximately 20 dB of isolation.

HP Package Outline 61 Cover Channel

The cover channel supplied with each diode should be used in balanced stripline circuits in order to provide good electrical continuity from the upper to the lower ground plane through the package base metal. Higher order modes will be excited if this cover is left off or if poor electrical contact is made to the ground plane.

The package transmission channel is filled with epoxy resin which combines a low expansion coefficient with high chemical stability.

Maximum Ratings at T_{CASE}=25°C

Part No. 5082-	-3140 -3170	-3141	-3040 -3340	-3041	-3046	-3071
Junction Operating and Storage Temperature Range	-65°C to 150°C	-65°C to 150°C	-65°C to 125°C	-65°C to 125°C		
Power Dissipation[1]	1.75 W	.75 W	2.5 W	1.0 W	4.0 W	1.0 W
Peak Incident Pulse Power[2]	225 W	50 W	225 W	50 W	2000 W	50 W
Peak Inverse Voltage	150 V	70 V	150 V	70 V	450 V	50 V
Soldering Temperature	230°C for 5 sec.					

Notes:

1. Device properly mounted in sufficent heat sink, derate linearly to zero at maximum operating temperature.
2. t_p = 1 μs, f = 10 GHz, Du - .001, Z_o = 50Ω. (Exception: -3071 is tested at 9.4 GHz.)

Electrical Specifications at $T_A = 25°C$ - Attenuator Diodes

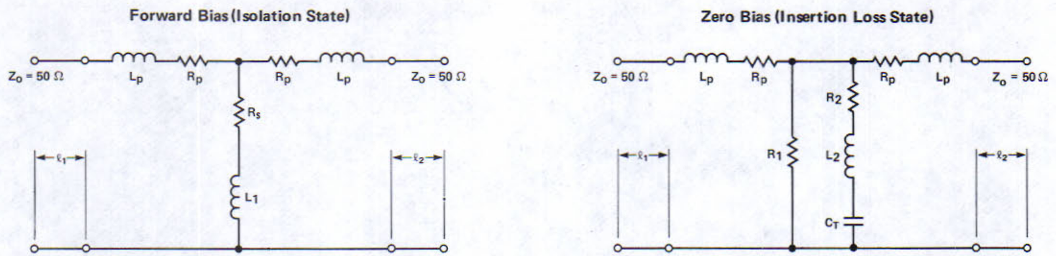
Part Number 5082-	Package Outline	Heat Sink	Minimum Isolation (dB)	Maximum Insertion Loss (dB)	Maximum SWR	Maximum Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
3140	60	Anode	20	0.5	1.5	–	400	30
3141	60	Cathode	20	1.0	1.5	10	15	13
3170	60	Cathode	20	0.5	1.5	–	400	30
3040	61	Anode	20	0.5	1.5	–	400	30
3041	61	Cathode	20	1.0	1.5	10	15	13
3046	61	Anode	20	1.0	1.5	–	1000	50
3340	61	Cathode	20	0.5	1.5	–	400	30
Test Conditions (Note 3)	–	–	I_F=100mA (Except 3041,3141; I_F=20mA)	I_F = 0 P_{in} = 1mW	I_F = 0 P_{in} = 1mW	I_F = 20mA V_R = 10V Recovery to 90%	I_F = 50mA I_R = 250mA	–

Note 3: Test Frequencies: 8 GHz 5082-3041, -3046 and -3141. 10 GHz 5082-3040, -3140, 3170 and -3340.

Electrical Specifications at $T_A = 25°C$ - Limiter Diode

Part Number 5082-	Package Outline	Heat Sink	Maximum Insertion Loss (dB)	Maximum SWR	Maximum RF Leakage Power (W)	Typical Recovery Time (ns)
3071	61	Cathode	1.2	2.0	1.0	100
Test Conditions	–	–	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 50 W	P_{in} = 50 W

Equivalent Circuits



Typical Equivalent Circuit Parameters - Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L_1 (pH)	ℓ_1 (mm)	ℓ_2 (mm)
3040, 3340	200	0.25	1.0	20	2.4	5.0
3041	220	0.25	1.0	20	2.4	5.0
3046	220	0.25	0.6	17	2.4	5.0
3140, 3170	150	0.0	0.95	30	3.8	3.8
3141	150	0.0	0.8	20	3.8	3.8

Typical Equivalent Circuit Parameters - Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R_1 (KΩ)	L_2 (pH)	R_2 (KΩ)	C_T (pF)	ℓ_1 (mm)	ℓ_2 (mm)
3040, 3340	200	0.25	∞	0	5.0	0.10	2.4	5.0
3041	220	0.25	∞	0	1.5	0.15	2.4	5.0
3046	220	0.25	∞	0	1.5	0.15	2.4	5.0
3140, 3170	30	0.0	1.2	16	0.0	0.20	5.3	5.3
3141	200	0.0	∞	0	0.4	0.14	4.4	4.4

Typical Parameters

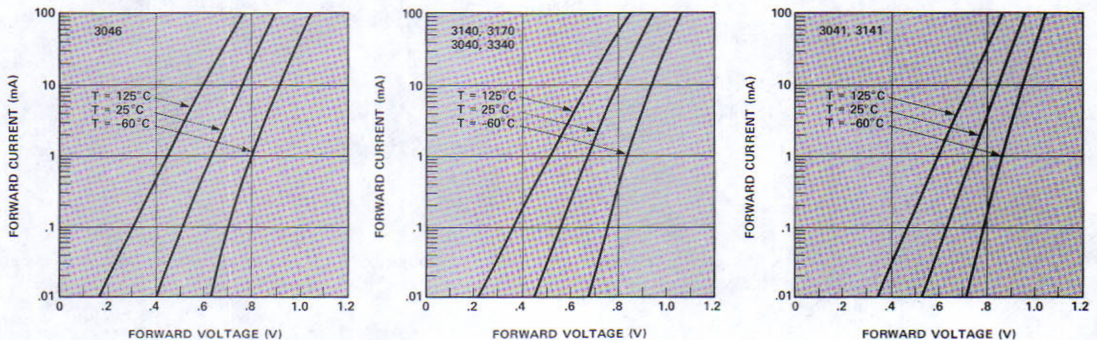


Figure 1. Typical Forward Characteristics.

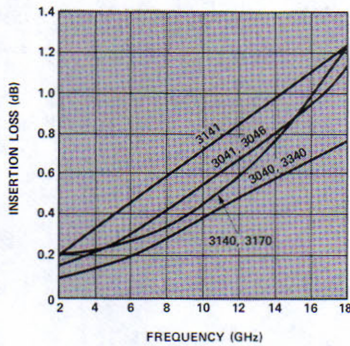


Figure 2. Typical Insertion Loss vs. Frequency.

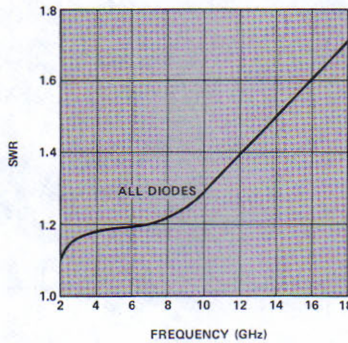


Figure 3. Typical SWR vs. Frequency.

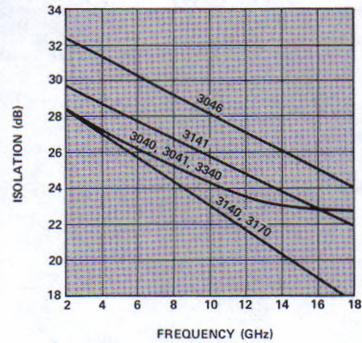


Figure 4. Typical Isolation vs. Frequency.

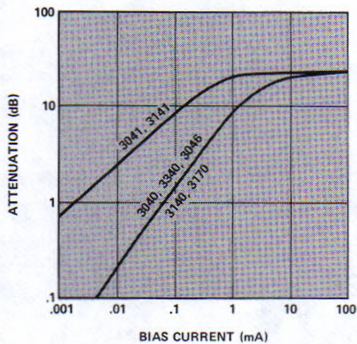


Figure 5. Typical Attenuation Above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.

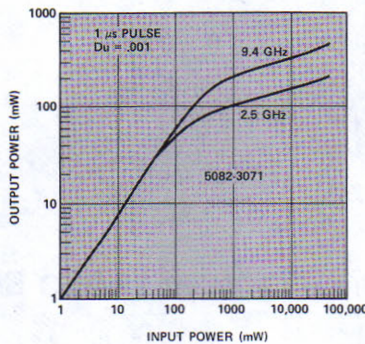
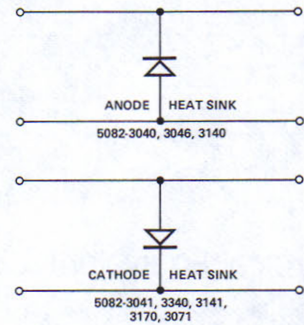


Figure 6. Typical Pulse Limiting Characteristics.



HEAT SINK POLARITY

DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 7. HP Package 60 Outline.

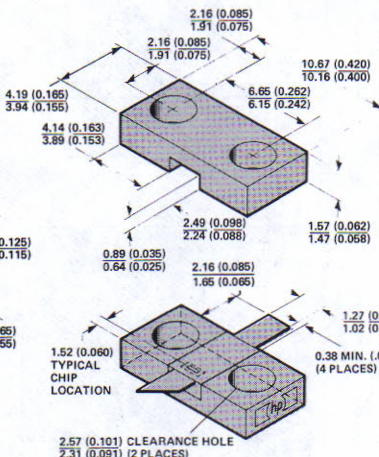


Figure 8. HP Package 61 Outline.

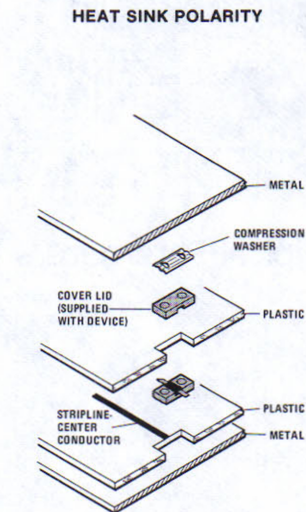


Figure 9. Suggested Stripline Assembly.

Typical Switching Parameters

RF SWITCHING SPEED

HP 5082-3141 and HP 5082-3041

The RF switching speed of the HP 5082-3141 and HP 5082-3041 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50Ω system is considered for two cases: one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second, driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 10. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

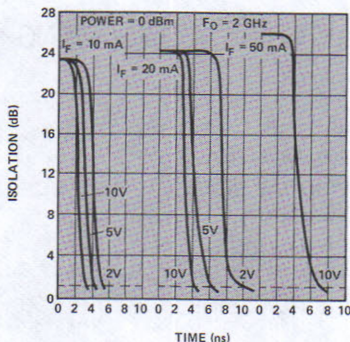


Figure 10. Isolation vs. Time (Turn-on) for HP 5082-3141 and HP 5082-3041. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929; Fast Switching PIN Diodes.

REVERSE RECOVERY TIME

Shown below is reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_R. The circuit used to measure t_{rr} is shown in Figure 11.

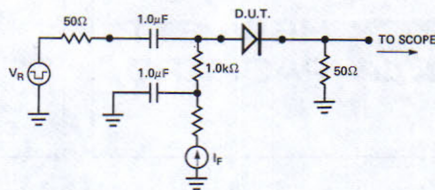


Figure 11. Basic t_{rr} Test Setup.

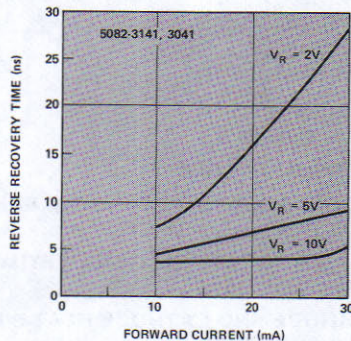


Figure 12. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3141, -3041.

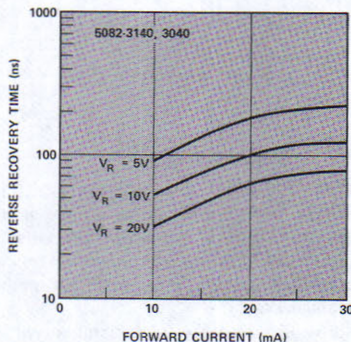


Figure 13. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3140, -3040.

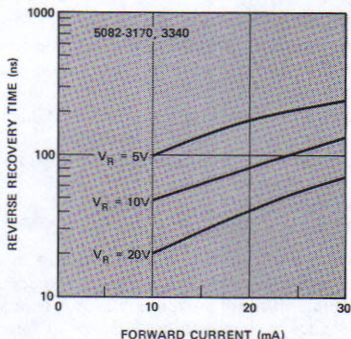


Figure 14. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3170, -3340.

HEWLETT PACKARD

PIN DIODES FOR FAST SWITCHING RF POWER SWITCHING AND ATTENUATION

5082-3101/02
5082-3201/02
5082-3303/04
5082-3305/06

RF POWER SWITCHING/ATTENUATING

Features

HIGH ISOLATION
Greater Than 25 dB

LOW INSERTION LOSS

HIGH CONTROL SIGNAL DYNAMIC RANGE
10,000: 1 RF Resistance Change

LOW HARMONIC DISTORTION LIFETIME
Greater Than 100 ns

BOTH ANODE AND CATHODE HEAT SINK MODELS AVAILABLE

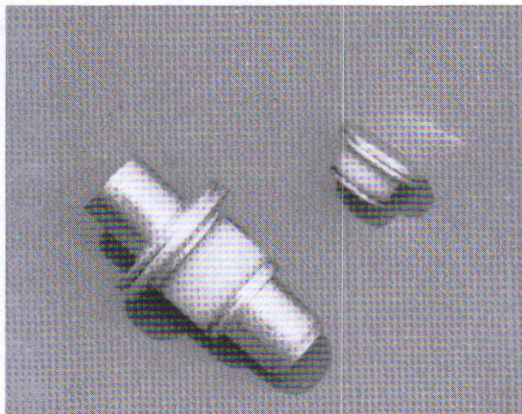
Description/Applications

HP 5082-3101/02, 5082-3201/02, 5082-3303/04 PIN diodes are silicon devices manufactured using modern processing techniques to provide optimum characteristics for RF switching, signal conditioning and control. These devices are of planar passivated design. Both anode and cathode heat sink models are available.

PIN diodes provide a variable RF resistance with DC bias current. The main advantages of a PIN diode over PN switching diodes are the low forward resistance and the low device capacitance.

These HP PIN Diodes are intended for use in RF switching, multiplexing, modulating, phase shifting, and attenuating applications from approximately 10 MHz to frequencies well into the microwave region. Due to their low parasitic capacitance and inductance, both HP Package Outline 31 and 38 are well suited for broadband circuits up to 1 GHz and for resonated circuits up to 8 GHz. Broad band designs above 1 GHz are usually more economical using stripline PIN diodes (HP Package Outlines 60 and 61) or devices for microstrip circuits (HP Package Outlines 72 and 74).

These devices are especially useful where the lowest residual series resistance and junction capacitance are required for high on-to-off switching ratios. At constant bias the RF resistance is relatively insensitive to temperature, increasing only 20% for a temperature change from +25°C to +100°C.



FAST SWITCHING/ATTENUATING

Features

NANOSECOND SWITCHING TIME
Typically Less Than 5 ns

LOW RESIDUAL SERIES RESISTANCE
Less Than 1Ω

LOW DRIVE CURRENT REQUIRED
Less Than 20 mA for 1Ω R_S

CATHODE HEAT SINK

Description/Applications

The HP 5082-3305 and 5082-3306 are passivated silicon PIN diodes of mesa construction. Precisely controlled processing provides an exceptional combination of fast RF switching and low residual series resistance.

These HP PIN diodes provide unique benefits in the high isolation to insertion loss ratio afforded by the low residual resistance at low bias currents and the ultra-fast recovery realized through lower stored charge. Where low drive power is desired these diodes provide excellent performance at very low bias currents.

The HP 5082-3305 and 5082-3306 ceramic package PIN diodes are intended for controlling and processing microwave signals up to Ku band. Typical applications include single and multi-throw switches, pulse modulators, amplitude modulators, phase shifters, duplexers, diplexers and TR switches.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range
.... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

DC Power Dissipation (Derate linearly to zero at 150°C)

HP 5082-3305 .... 0.7 W
HP 5082-3306 .... 1.25W
HP 5082-3101, 3102 .... 1.0 W
HP 5082-3201, 3202, 3303, 3304 .... 3.0 W

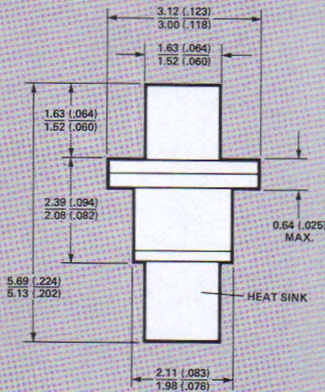
Mechanical Specifications

The HP Package Outline 31 has a metal ceramic hermetic seal. The heat sink stud is gold-plated copper. The opposite stud is gold-plated kovar. Typical package inductance is 1.0 nH and typical package capacitance is 0.2 pF.

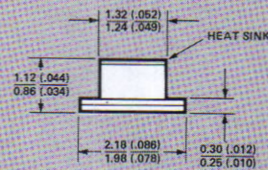
The HP Package Outline 38 also has a metal ceramic hermetic seal. The heat sink contact is gold plated copper. The opposite contact is gold-plated kovar. Typical package inductance is 0.4 nH and typical package capacitance is 0.2 pF.

The maximum soldering temperature for diodes in either package is 230°C for 5 seconds.

Package Dimensions



Outline 31



Outline 38

DIMENSIONS IN MILLIMETERS AND (INCHES).

PIN Diodes

RF POWER SWITCHING/ATTENUATING

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR}	Maximum Total Capacitance C_T	Maximum Residual Series Resistance R_S	Minimum Carrier Lifetime τ	Typical Reverse Recovery Time t_{rr}	Typical CW Power Handling Capability P_A
3101	38	Anode	200	0.32	1.2	100	100	40
3102	38	Anode	300	0.30	0.8	100	100	60
3201	31	Anode	200	0.35	1.2	100	100	120
3202	31	Anode	300	0.32	0.8	100	100	180
3303	31	Cathode	200	0.40	1.2	100	100	120
3304	31	Cathode	300	0.32	0.8	100	100	180
Units			V	pF	Ω	ns	ns	W
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leqslant 10\mu A$	$V_R = 50V$, $f = 1MHz$	$I_F = 100mA$ $f = 100MHz$	$I_F = 50mA$ $I_R = 250mA$	$I_F = 20mA$, $V_R = 10V$ 90% Recovery	Series* Switch in 50Ω System

*Divide by four for a shunt switch.

FAST SWITCHING/ATTENUATING

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR}	Maximum Total Capacitance C_{VR}	Maximum Series Resistance R_S	Maximum Reverse Recovery Time t_{rr}
3305	38	Cathode	70	0.4	1.0	10.0
3306	31	Cathode	70	0.45	1.0	10.0
Units			V	pF	Ω	ns
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leqslant 10\ \mu A$	$f = 1\ MHz$ $V_R = 20V$	$f = 100\ MHz$ $I_F = 20mA$	$I_F = 20mA$ $V_R = 10V$ 90% Recovery

FAST SWITCHING/ATTENUATING
Typical Parameters (5082-3305 and -3306)

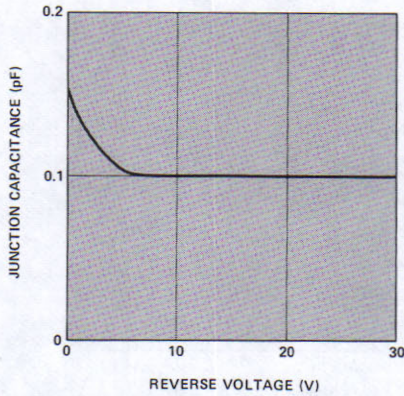


Figure 1. Typical Junction Capacitance vs. Reverse Voltage.

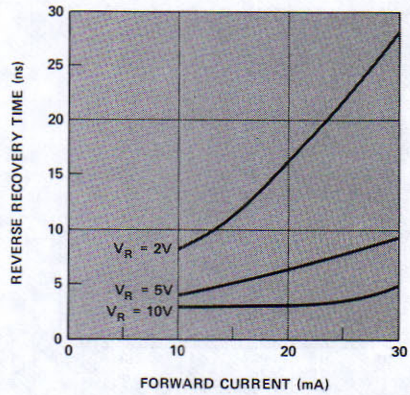


Figure 2. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages. For further discussion of switching characteristics, see 5082-3041 data sheet.

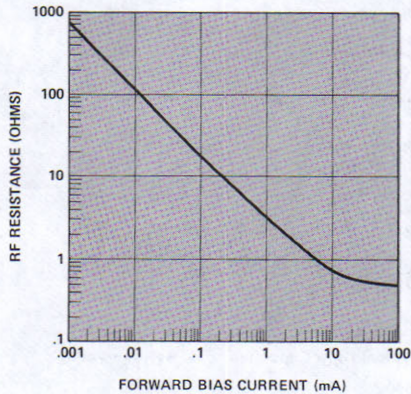


Figure 3. Typical RF Resistance vs. Forward Bias Current.

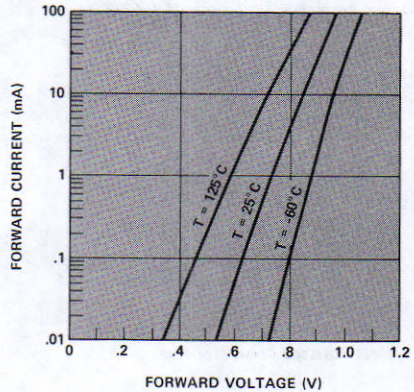


Figure 4. Typical Forward Current vs. Forward Voltage.

PIN Diodes

RF POWER SWITCHING/ATTENUATING

Typical Parameters (5082-3101, -3102, -3201, -3202, -3303, -3304)

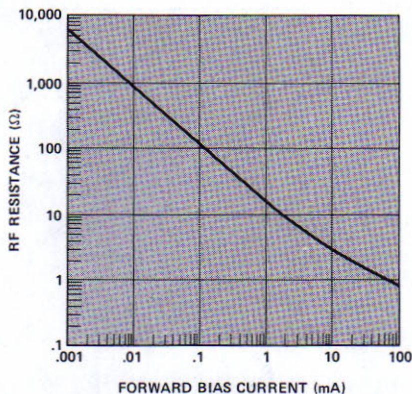


Figure 5. Typical RF Resistance vs. Forward Bias Current.

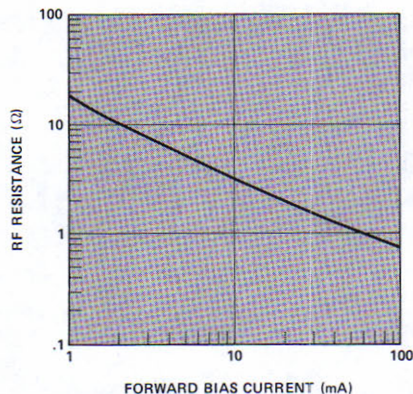


Figure 6. Typical RF Resistance vs. Forward Bias Current.

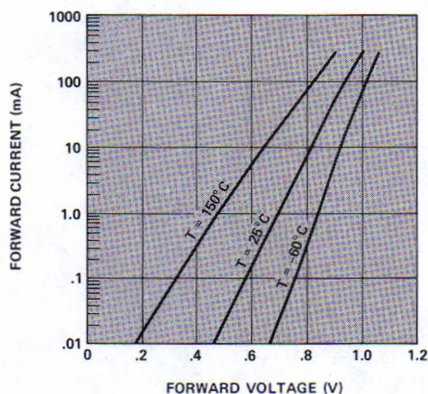


Figure 7. Typical Forward Characteristics.

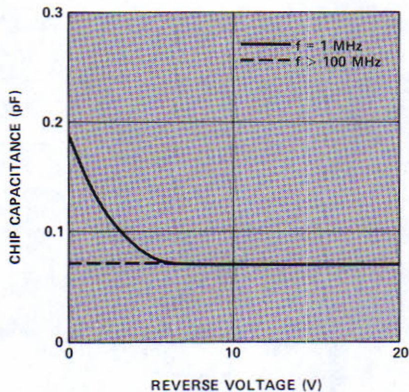
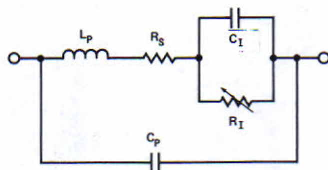


Figure 8. Typical Chip Capacitance vs. Reverse Voltage.



C_P = Package Capacitance
L_P = Package Inductance
R_S = Residual Series Resistance
R_I = I-Layer Resistance
C_I = I-Layer Capacitance

TYPICAL VALUES FOR C_P AND L_P ARE GIVEN UNDER "MECHANICAL SPECIFICATIONS". WITH REVERSE BIAS, $R_I \cong 10k\ \Omega$. TOTAL CAPACITANCE IS C_T AND IS GIVEN IN "ELECTRICAL SPECIFICATIONS". WITH FORWARD BIAS C_I IS NO LONGER PRESENT. R_I DECREASES WITH INCREASING FORWARD BIAS TO APPROXIMATELY ZERO AT 100 mA.

Figure 9. Device Equivalent Circuit.

HEWLETT PACKARD

HIGH CONDUCTANCE DIODES

5082-1001
5082-1002
5082-1006

PIN Diodes

Features

FAST SWITCHING
LOW CAPACITANCE
HIGH CURRENT CAPABILITY

Description/Applications

The 5082-1000 series of diodes feature planar silicon epitaxial construction to provide high conductance, low capacitance, and nanosecond turn-on and turn-off. Process control of the diode manufacturing enables specification of effective minority carrier lifetime. Turn-on time and voltage overshoot are minimized in these diodes of low conductivity modulation.

These diodes are ideally suited for applications such as core drivers, pulse generators, input gates or wherever high conductance without loss of speed is required.

Maximum Ratings at $T_{CASE} = 25°C$

WIV — Working Inverse Voltage
- 1006 .... 40 Volts
- 1001/1002 .... 30 Volts

I_F (Surge) — Forward Current Surge, 1.0 Second Duration .... 0.75 Amp

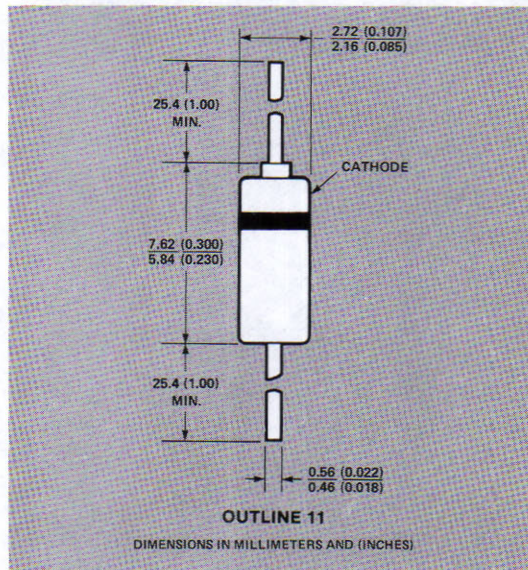
I_F (Surge) — Forward Current Surge, 1.0 Microsecond Duration .... 7.50 Amp

P_{DISS} — Power Dissipation[1] .... 500 mW

T_A — Operating Temperature Range -65°C to +175°C

T_{STG} — Storage Temperature Range -65°C to +200°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.



OUTLINE 11

DIMENSIONS IN MILLIMETERS AND (INCHES)

Mechanical Specifications

The HP Outline 11 package has a glass hermetic seal with dumet leads. The package will meet MIL-STD-750, Method 2036, Condition A (2 lbs. tension for 15 sec.) and E. The maximum soldering temperature is 230°C for 5 seconds. Outline 11 package capacitance and inductance are typically 0.15 pF and 4 nH respectively.

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Minimum Breakdown Voltage V_{BR} (V)	Minimum Forward Current I_F (mA)	Minimum Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA)	Maximum Reverse Leakage Current I_R (μA)	Maximum Total Capacitance C_O (pF)	Maximum Reverse Recovery Time t_{rr} (ns)	Maximum Turn-On Time t_{on} (ns)
1001	35	150	500	200	200	1.5	1.5	2.5
1002	35	300	800	200	200	3.0	2.0	2.5
1006	50	150	500	200	200	1.1	1.5	—
Test Conditions	$I_R = 10 \mu A$	$V_F = 1.0V$ [2]	$V_F = 1.4V$ [2]	[3]	150°C [3]	$V_R = 0V$, f=1.0 MHz	(Figure 9)	(Figure 10)

NOTES:
1. Mounted on a printed circuit board in still air.
2. Measured at a repetition rate not to exceed the power dissipation.
3. $V_R = 35V$ for 1006; $V_R = 30V$ for 1001, 1002.
4. Inductance measured at the edge of the glass package seal is typically 4.0 nH for all devices.
5. Rectification Efficiency is typically 65% for all devices (Figure 8).

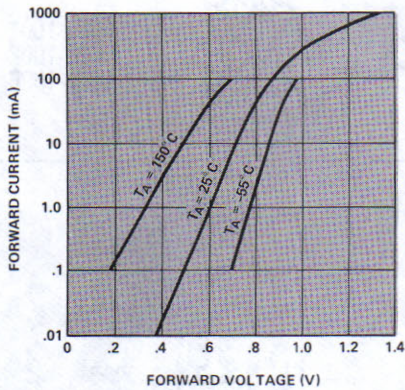


Figure 1. Typical Forward Conduction Characteristics. 5082-1001 and 1006.

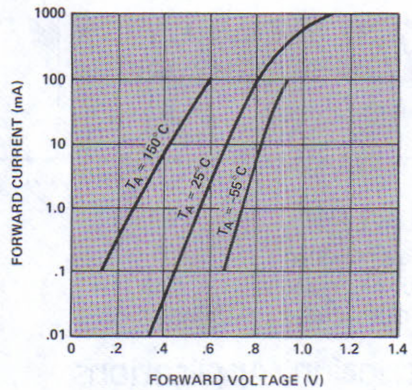


Figure 2. Typical Forward Conduction Characteristics. 5082-1002.

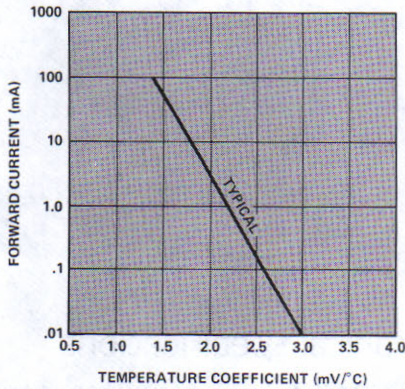


Figure 3. Typical Forward Current Temperature Coefficient.

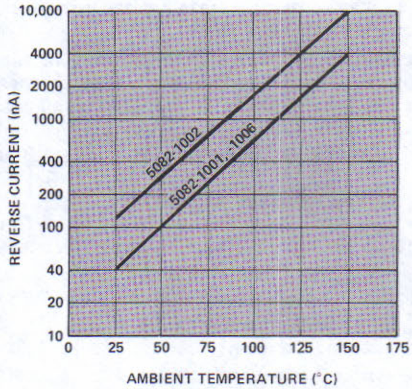


Figure 4. Typical Reverse Current at Specified V_R vs. Increasing Temperature.

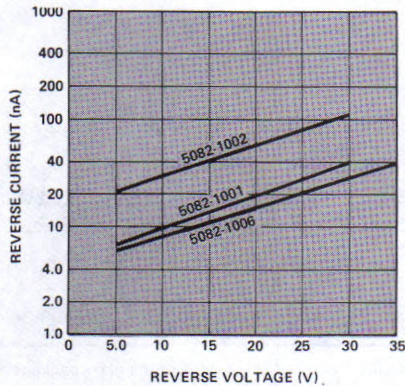


Figure 5. Typical Reverse Current vs. Reverse Voltage.

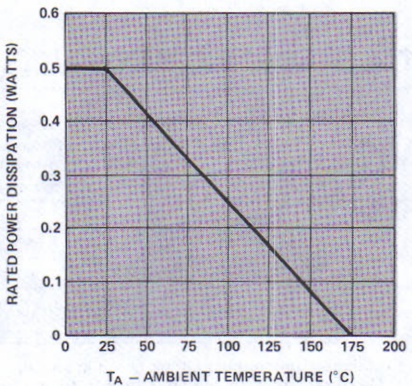


Figure 6. Power Dissipation Derating Characteristics.

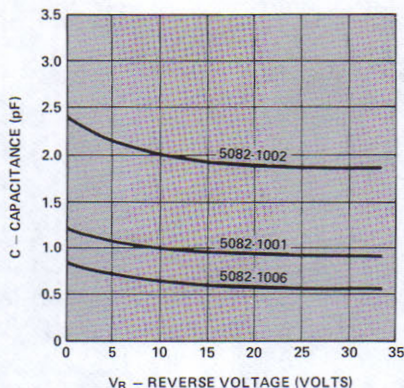


Figure 7. Typical Capacitance vs. Reverse Voltage Characteristics.

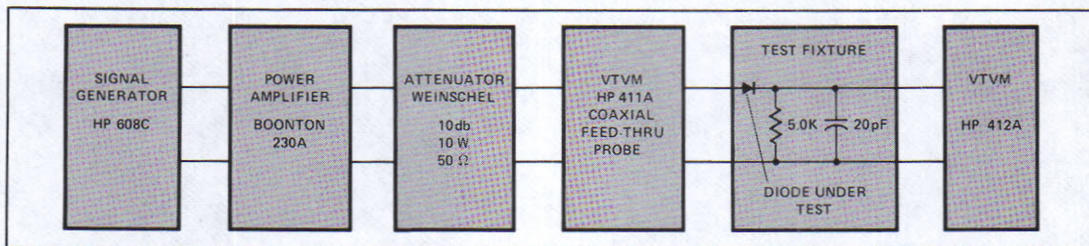


Figure 8. Test Circuit for Measuring the Rectification Efficiency. Signal source is adjusted to 100 MHz and 2V RMS as read on the 411A. The rectification efficiency calculated from the DC output voltage by RE = $V_{DC}/2.83$ is typically 65% for all devices.

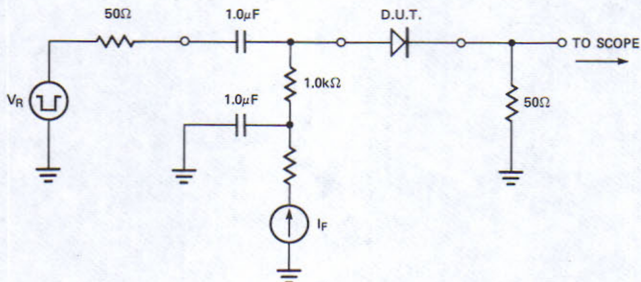


Figure 9. Test Circuit for Measuring Reverse Recovery Time. I_F is set at 20 mA and V_R at 2V.

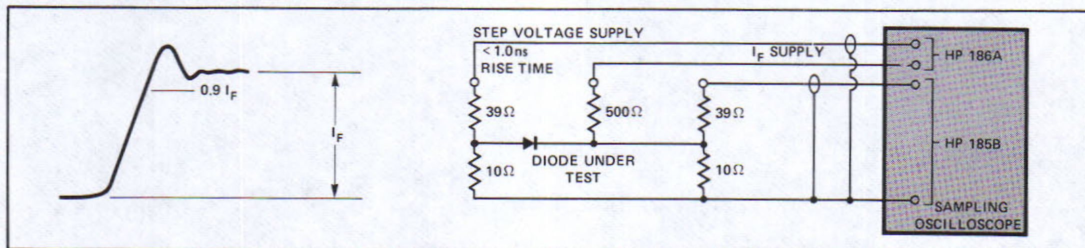


Figure 10. Test Circuit for Measuring Turn-On Time. I_F is adjusted for 10 mA after applying the step voltage. t_{ON} is measured as the time required to reach 0.9 I_F from initial application of the step voltage. For high excitation levels the t_{ON} value is significantly lower than the value specified, i.e., at 100 mA t_{ON} is typically less than 1.0 ns.

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PIN Diode RF Resistance Measurement 152

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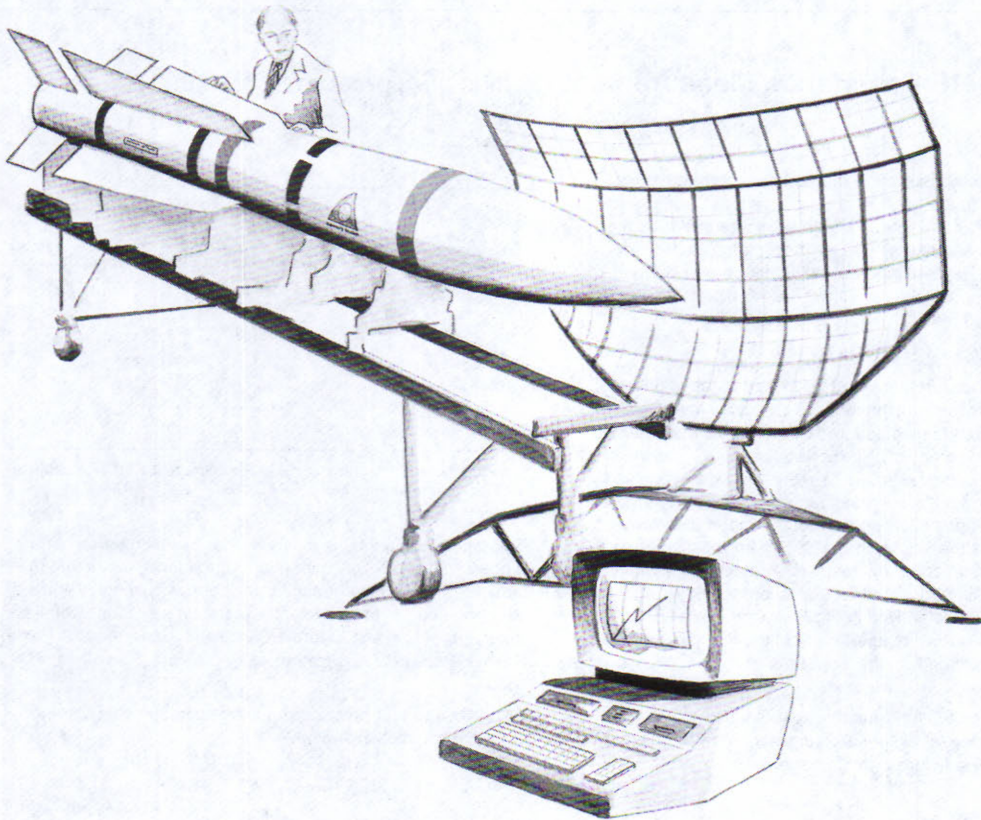
PIN Diodes



HEWLETT PACKARD

APPLICATIONS FOR PIN DIODES

Applications of PIN Diodes (Portion of Application Note 922)

The most important property of the PIN diode is the fact that it appears as an almost pure resistance at RF whose resistance value can be varied over a range of approximately 1 to 10,000 ohms by a direct or low frequency control current.

When the control current is varied continuously, the PIN diode is useful for attenuating, leveling and amplitude modulating an RF signal. When the control current is switched "on" and "off" or in discrete steps, the device is useful for switching, pulse modulating, and phase shifting of an RF signal.

In addition, the PIN's small size, weight, high switching speed, and freedom from parasitic elements make it ideally suited for use in miniature, broadband RF signal control components.

This application note describes the important properties of the PIN diode and illustrates how it can be applied in a variety of RF control circuits. Topics discussed include the following:

Characteristics of the PIN Diode
- (a) Low and High Frequency Equivalent Circuits
- (b) The RF Resistance Characteristic
- (c) Effects of Package Parasitics

PIN Diode Applications
- (a) Design of Broadband Reflective Switches and Attenuators
- (b) Design of Resonant Switches
- (c) Design of Multiple Diode and Multi-throw Switches and Attenuators
- (d) Design of Constant Impedance Switches and Attenuators
- (e) PIN Diode Phase Shifters

PIN Diode Power Handling

PIN Diode RF Resistance Measurement (Portion of Application Bulletin 6)

INTRODUCTION

In order to correctly determine the resistance characteristic of a PIN diode, several test methods have been suggested and devised by various sources. Many of these methods are inaccurate or time-consuming. This Application Bulletin describes how the RF resistance of a PIN diode can be measured reliably and efficiently with the use of the HP 4815 Vector Impedance Meter.

RF RESISTANCE MEASUREMENT

The resistance measurement method to be described utilizes a tunable fixture to tune out the reactive part of the impedance, leaving the real part to be measured by the Vector Impedance Meter. A block diagram of the test equipment is shown in Fig. 1. The diode under test (D.U.T.) in the test fixture receives the proper bias from the current source. The fixture is tuned for a zero phase indication on the Vector Impedance Meter. The resistance is then read on the Vector Impedance Meter or (for better resolution at low resistance levels) on a Digital Voltmeter which is connected to the recorder output of the Vector Impedance Meter. Use of the Precision Power Source to provide a stable low voltage for offsetting the short circuit resistance is described in the Appendix of this Application Bulletin.

With some diodes a single tunable test fixture will tune out the diode reactance for all forward currents. For other diodes more than one test fixture may be necessary.

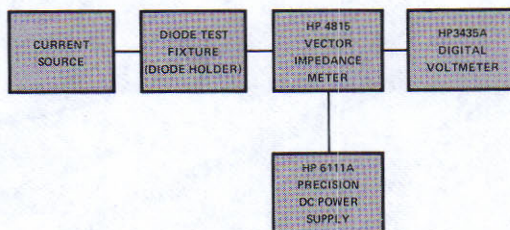


Figure 1. Block Diagram of Test Equipment for RF Resistance Measurement of a PIN Diode.

The test fixture contains a circuit (Fig. 3) which tunes out the diode reactance. The essential components are a tunable inductor and tunable capacitor in the tuning section and an RF choke and bypass capacitor in the bias section. Detailed drawings of this test fixture are available upon request from Hewlett-Packard, Applications Department, San Jose, CA 95131.

Details of the test procedure are contained in the Appendix of this Application Bulletin.

Power Handling Capability of PIN Diode Switches and Attenuators

This summary of equations for power handling calculations is intended to provide the tools for a first order analysis of the RF power handling capability of switches, phase shifters, or attenuators. It is assumed that parasitic circuit elements are negligible or tuned out.

Summary of Symbols:

- P_A — Power in transmission line (maximum available power to load).
- P_R — Power dissipated in PIN diode, may be as high as P_{DISS} max specified for the device under consideration.
- R — Resistance of PIN diode in "on" or "off" condition, whichever creates higher P_R.
- V_{BR} — Breakdown voltage of PIN diode.
- V_R — Reverse bias applied to diode.
- A — Attenuation ratio of series or parallel diode inserted into transmission line.

CALCULATION SEQUENCE:

1. Read P_{DISS} max from the absolute maximum ratings.
2. Determine the CW Power Multiplier from Equation (1) for a shunt circuit, or Equation (4) for a series circuit. Alternatively, Figure 3 can be used if diode resistance is known, or Figure 4 can be used if circuit attenuation is known.
3. Multiply P_{DISS} max by the CW Power Multiplier to determine CW power handling capability.
4. Check for peak power handling limit due to V_{BR} by using Equation (3) for shunt circuits and Equation (6) for series circuits, or the curves in Figure 5.

Shunt Circuit

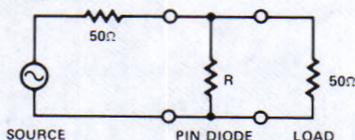


Figure 1. Shunt Attenuator/Switch Circuit.

Power Multiplier: $$\frac{P_A}{P_R} = \frac{(25 + R)^2}{50R} \qquad (1)$$

Attenuation: $$A = 20 \log_{10} \left(1 + \frac{25}{R}\right), \text{dB} \qquad (2)$$

Breakdown Voltage Limit: $$P_A\,(\text{max}) = \frac{(V_{BR} - V_R)^2}{100}, \text{W} \qquad (3)$$

Series Circuit

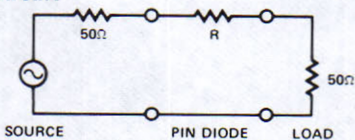


Figure 2. Series Attenuator/Switch Circuit.

Power Multiplier: $$\frac{P_A}{P_R} = \frac{(100 + R)^2}{200R} \qquad (4)$$

Attenuation: $$A = 20 \log_{10} \left(1 + \frac{R}{100}\right), \text{dB} \qquad (5)$$

Breakdown Voltage Limit: $$P_A\,(\text{max}) = \frac{(V_{BR} - V_R)^2}{400}, \text{W} \qquad (6)$$

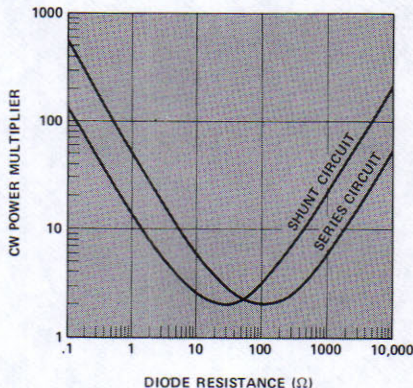


Figure 3. CW Power Multiplier vs. Diode Resistance.

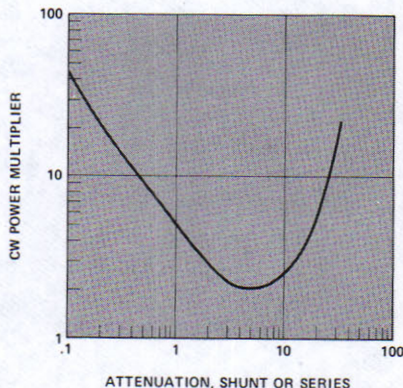


Figure 4. CW Power Multiplier vs. Series or Shunt Attenuation.

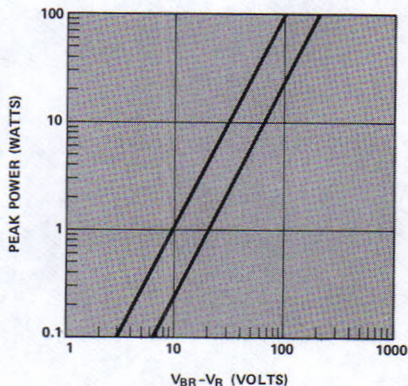


Figure 5. Power Handling Limit Due to Reverse Breakdown Voltage and Reverse Bias Voltage.

PIN Diodes

Step Recovery Diodes

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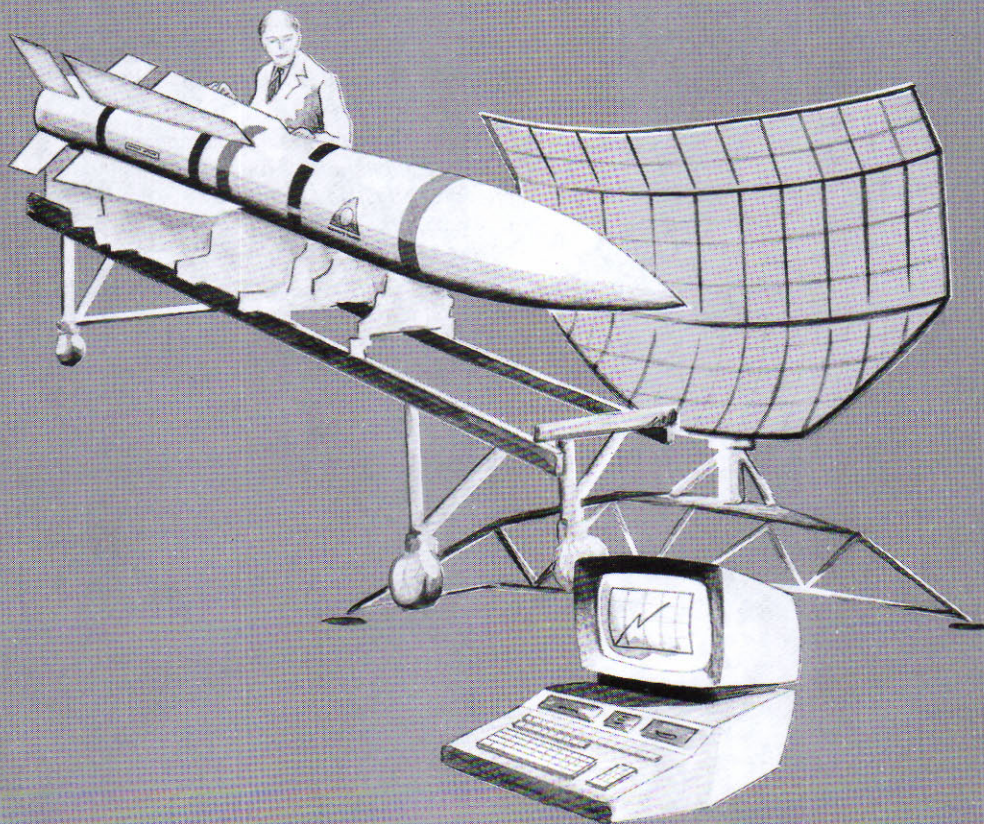
Selection Guide 157
Step Recovery Diodes 158



Step Recovery Diodes

Step Recovery Diodes are three layer devices, similar to PIN diodes, with a special treatment of the semiconductor to make the resistance change suddenly from a low to a high value as the charges are gradually withdrawn. Conventional PIN diodes are designed to have a gradual change of resistance for attenuator applications. The abrupt change of resistance is responsible for a spike of voltage equivalent to a comb of harmonics of the input frequency.

Diode Types

This catalog shows three types of Step Recovery Diodes. The high efficiency multiplier diodes are the most recently developed type. They have lower series resistance, hence better multiplying efficiency. Maximum output frequency is limited to approximately the inverse of the transition time and minimum input frequency to approximately the inverse of the lifetime.

The DC tested diodes are also efficient multipliers. They come from a more mature product line.

The other type of diode, the RF tested diode, is 100% tested to meet a minimum power output requirement in a production test multiplier. Output frequencies of 2, 6, 10 or 16 GHz are used in this test.

Multiplier Design

The design of multiplier circuits can be quite involved. A straight-forward design technique treats the input circuit as a low pass filter matching the diode model to the generator. Similarly, the output circuit is a bandpass filter matching the diode model to the load resistance. The model is a resistor in series with a capacitor. The capacitance value is double the reverse bias junction capacitance shown in the catalog (C_{-V}). The resistance is

$$\frac{A}{2\pi f_{in} C_{-V}}$$

where f_{in} is the input frequency and A is given in the following table for different multiplication factors, n.

n	2	4	6	8
A	0.21	0.042	0.018	0.010

Supplementary readings:

F. Ghoul, L. Besser and Chi Hsieh, *"Design a High Power S Band Doubler"*, Microwaves, June 1974, pp. 58-65

C.P. Burkhardt, *"Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Level"*, BSTJ, vol. 44, no. 4, April 1965, pp. 675-692

Step Recovery Diodes Selection Guide

Typical Output Frequency Range GHz	High Efficiency Multiplier Versions 5082-	RF Tested Versions 5082-	DC Tested Versions 5082-
1-3	0800	0300	0241
3-5	0805		0132
5-8	0810	0310	0132
7-10	0820, 0821	0320	0243
8-12	0830	0320	0253
10-20	0835, 0885	0335	

MIC versions shown on page 163 of Hybrid Section.

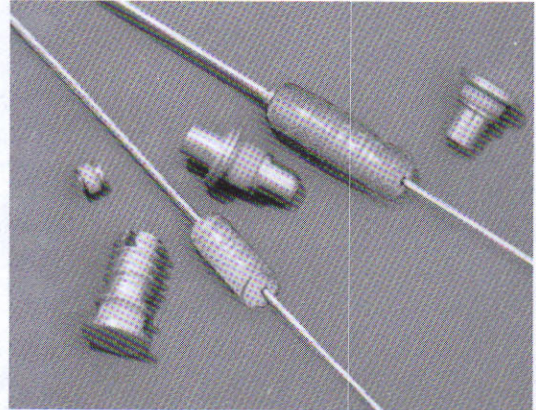
HEWLETT PACKARD

STEP RECOVERY DIODES

5082-0100 SERIES
5082-0200 SERIES
5082-0300 SERIES
5082-0800 SERIES

Features

- **OPTIMIZED FOR BOTH LOW AND HIGH ORDER MULTIPLIER DESIGNS FROM UHF THROUGH Ku BAND**
- **PASSIVATED CHIP FOR MAXIMUM STABILITY AND RELIABILITY**
- **AVAILABLE IN A VARIETY OF PACKAGES**



Description/Applications

These diodes are manufactured using modern epitaxial growth techniques. The diodes are passivated with a thermal oxide for maximum stability. The result is a family of devices offering highly repeatable, efficient and reliable performance. These diodes are designed to meet the general requirements of MIL-S-19500.

The 5082-0800 Series diode is designed to maximize cut-off frequency while maintaining a fast transition time. This characteristic leads to excellent performance in either low or high order multipliers and in comb generators. All ceramic package diodes in the 5082-0800 Series are supplied with measured data.

Maximum Ratings at $T_{CASE} = 25°C$

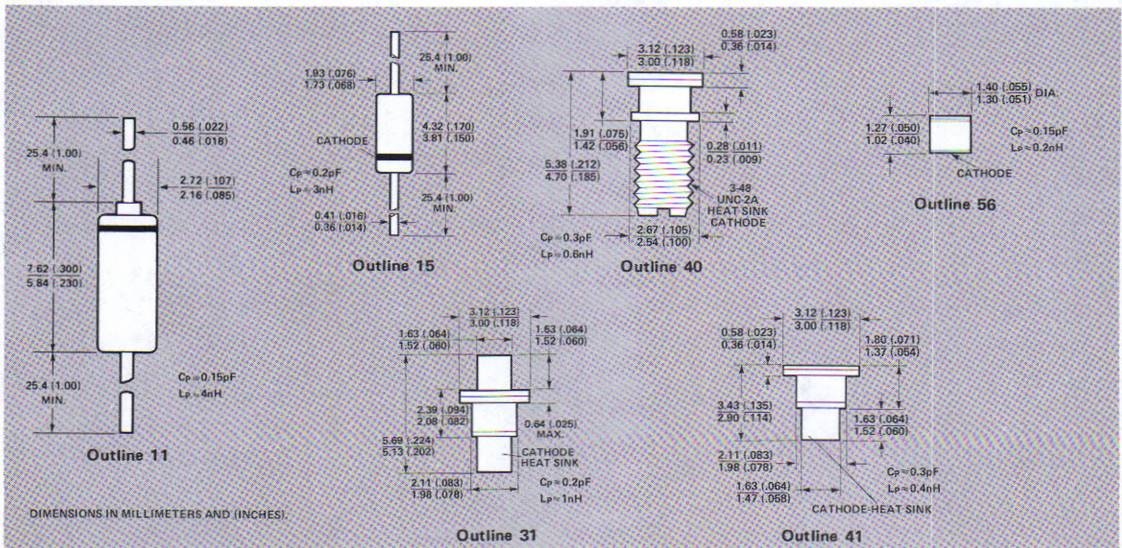
Junction Operating and
Storage Temperature .... -65°C to 200°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

DC Power Dissipation .... $\frac{200°C - T_{case}}{\theta_{jc}}$

Soldering Temperature .... 230°C for 5 sec.

Package Dimensions



Package Characteristics

Hewlett-Packard's step recovery diodes are available in a variety of packages.

The metal-ceramic packages are hermetically sealed. The anode studs and flanges are gold-plated Kovar. The cathode studs are gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

The HP outline 15 and 11 packages have glass hermetic seals with dumet leads. The maximum soldering temperature is 230°C for 5 seconds. The leads on outline 15 should be restricted so that any bend starts at least 1.6 mm (.063 in.) from the glass body.

Diodes for High Efficiency Multipliers (All Specifications at T_A = 25°C)

Ceramic Packaged Diodes

ELECTRICAL SPECIFICATIONS / TYPICAL PARAMETERS

Part Number 5082-	Junction Capacitance at -5V $C_{j(-6)}$[pF] f = 1 mHz Min.	Max.	Minimum Breakdown Voltage, V_{BR} at I_R = 10 μA [V]	Minimum Cutoff Frequency, f_c[1] [GHz]	Package Outline	Output Frequency Range [GHz]	Output Power, P_o[2] [W]	Lifetime τ [ns]	Transition Time t_t [ps]	Charge Level [pC]	Thermal Resistance Θ_{jc} [°C/W]
0800	3.5	5.0	75	100	40	1-3	10	250	350	1500	15
0805	2.5	3.5	60	140	31	3-5	6	100	250	1500	20
0810	1.5	2.5	60	140	31	5-8	4	100	200	1000	25
0820 0821	0.7	1.5	45	160	31 41	7-10	2.5	50	100	300	30
0830	0.35	1.2	25	200	31	8-12	1.0	25	75	300	45
0835 0885	0.1	0.5	15	350	31 56	10-20	0.3	15	60	100	60

Glass Packaged Diodes (Outline 15)[3]

ELECTRICAL SPECIFICATIONS / TYPICAL PARAMETERS

Part Number 5082-	Maximum Junction Capacitance at -6V, $C_{j(-6)}$ [pF]	Minimum Breakdown Voltage, V_{BR} at I_R = 10μA [V]	Minimum Cutoff Frequency, f_c [1] [GHz]	Lifetime, τ [ns]	Transition Time t_t [ps]	Charge Level [pC]
0803	6.0	70	100	250	350	1500
0815	4.0	50	140	100	250	1500
0825	2.0	45	160	50	100	300
0833	1.6	25	175	25	75*	300
0840	0.6	15	30u	15	60*	100

*The transition times shown for the package 15 devices are limited by the package inductance to a minimum of 100 ps. The lower transition times shown for the -0833 and -0840 are based on the performance of the chip.

RF Tested Diodes (All Specifications at T_A = 25°C)

ELECTRICAL SPECIFICATIONS / TYPICAL PARAMETERS

Part Number 5082-	Output Frequency, f_o [GHz]	N Order	Minimum Output Power, P_o[4] [W]	Junction Capacitance at −10V, C_j [pF]		Breakdown Voltage at I_R=10µA V_{BR} [V]		Maximum Thermal Resistance, θ_{jc} [°C/W]	Package Outline	Transition Time		Lifetime, τ [ns]
				Min.	Max.	Min.	Max.			t_t [ps]	Charge Level [pc]	
0300	2	X 10	2.0	3.2	4.7	75	100	14	40	300	2400	200
0310	6	X 10	0.4	1.6	2.7	40	60	30	41	160	1000	75
0320	10	X 5	0.23	0.35	1.0	25	40	60	41	75	300	25
0335	16	X 8	0.03	0.25	0.5	20	30	75	31	60	100	15

DC Tested Diodes (All Specifications at T_A = 25°C)

ELECTRICAL SPECIFICATIONS / TYPICAL PARAMETERS

Part Number 5082-	Maximum Junction Capacitance at -10V, $C_{j(-10)}$[pF] f = 1 mHz	Minimum Breakdown Voltage at I_R=10µA V_{BR} [V]	Maximum Transition Time		Package Outline	Lifetime τ [ns]	Thermal Resistance Θ_{jc} [°C/W]
			t_t [ps]	Charge Level [pC]			
0113	4.85	35	250	1500	11	100	300
0241	4.6	65	275	1500	31	150	20
0180	4.45	50	225	1500	11	150	300
0114	3.85	35	225	1500	11	100	300
0112	1.55	35	175	1000	11	50	300
0132	1.5	35	175	1000	31	50	40
0243	1.2	35	110	600	31	40	50
0151	0.65	15	90	200	15	20	600
0253	0.6	25	80	200	31	20	75
0153	0.4	25	90	200	15	20	600

Suggested output frequency, $f_{o(max)} \leqslant 1/t_t$

NOTES:
1. $f_c = \dfrac{1}{2\pi R_s C_{j(-6)}}$
2. As a doubler at midband.
3. For package outline 15 typical thermal resistance is 600° C/W with adequate heat sink.
4. Guaranteed multiplier tested results. Input power is: 5082-0300 15W; 5082-0310 4W; 5082-0320 2W; 5082-0335 0.65W

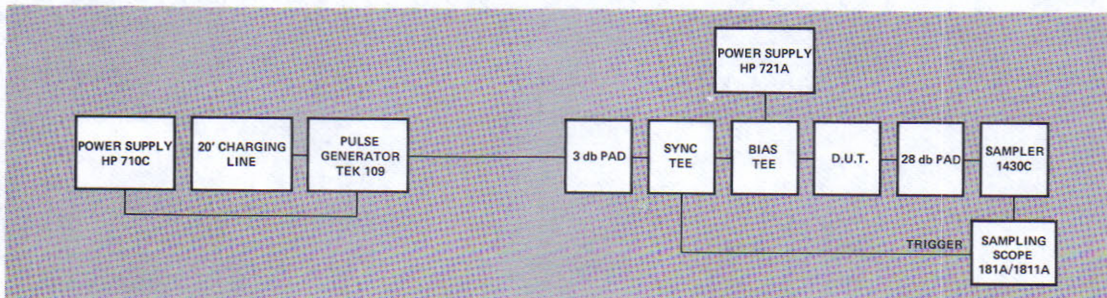


Figure 1. Test circuit for transition time. The pulse generator circuit is adjusted for a 0.5 A pulse when testing 5082-0151, 0253, 0335, 0835, 0885 and 0840. A pulse of 1.0 A is used for all other diodes. The bias current is adjusted for the specified stored charge level. The transition time is read between the 20% and the 80% points on the oscilloscope.

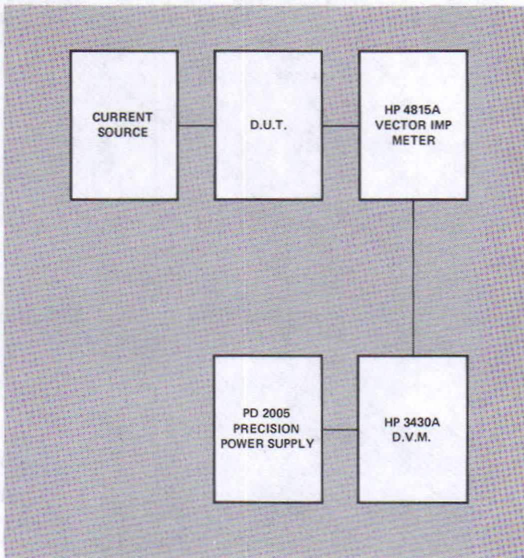


Figure 2. Test set-up for measurement of series resistance. The D.U.T. is forward biased (I_F) and the real part of the diode impedance is measured at 100 MHz. The D.V.M. is set up to read the real part on the Vector Voltmeter. The precision power supply is used to offset the test circuit resistance. R_S is measured at I_F = 100mA except 0800, 0801, 0802, 0803 where I_F = 500mA.

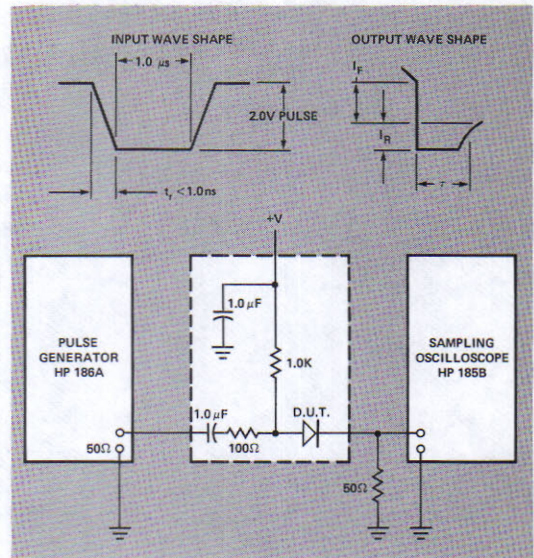


Figure 3. The Circuit for Measurement of the Effective Minority Carrier Lifetime. The value of the reverse current (I_R) is approximately 6 mA and the forward current (I_F) is 1.71 I_R. The lifetime (τ) is measured across the 50% points of the observed wave shape. The input pulse is provided by a pulse generator having a rise time of less than one nanosecond. The output pulse is amplified and observed on a sampling oscilloscope.

Step Recovery Diodes

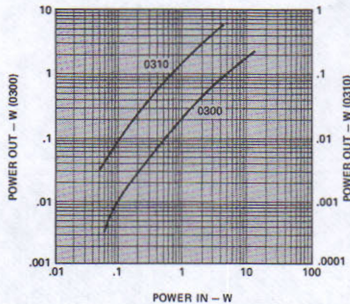


Figure 4. Typical Output Powers vs. Input Power at T_A = 25°C. The 5082-0300 is measured in a x 10 multiplier with P_{IN} at 0.2 GHz and P_O at 2.0 GHz. The 5082-0310 is measured in a x 10 multiplier with P_{IN} at 0.6 GHz and P_O at 6.0 GHz.

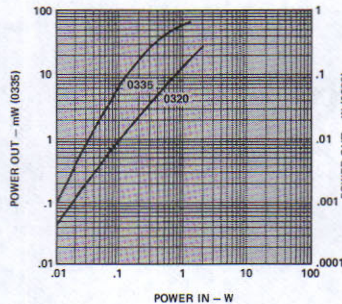


Figure 5. Typical Output Power vs. Input Power at T_A = 25°C. The 5082-0335 is measured in a x 8 multiplier with P_{IN} at 2 GHz and P_O at 16 GHz. The 5082-0320 is measured in a x 5 multiplier with P_{IN} at 2.0 GHz and P_O at 10 GHz.

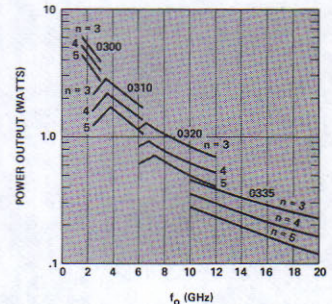


Figure 6. Predicted power output curves for 03XX step recovery diodes in X3, X4, and X5 multiplier applications. These results were obtained using computer organization programs.

Devices for Hybrid Integrated Circuits

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Gallium Arsenide Field Effect Transistors

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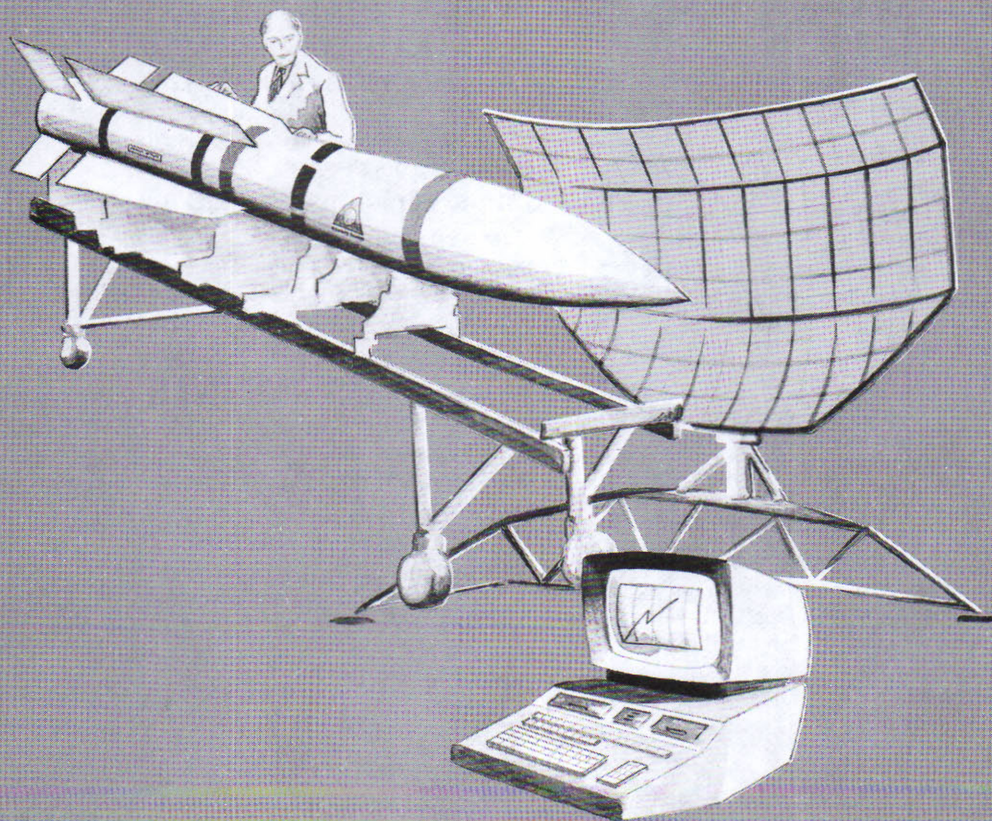


Beam Lead and Chip Devices for Hybrid Integrated Circuits

The move to smaller and lighter equipment continues for both military and non-military systems. As a result the market for hybrid integrated circuits is growing more rapidly than the market for waveguide and coaxial circuits. For the convenience of designers in this medium, the devices that are suitable for hybrid integrated circuits are shown in this section of the catalog.

The smallest and most popular outline for this application is the beam lead diode. Anode and cathode leads are deposited on the silicon wafer and become an integral part of the diode. These leads can be attached to the circuit by thermocompression bonding. Lead inductance is about 0.1 nH. This is less than half the inductance of a wire bond to a chip. Low parasitics are especially valuable in broad band circuits.

Figure 1 shows a beam lead diode quad (5082-9399) bonded on a carrier. The leads lie flat on the circuit and the bond is centered on the lead. These features indicate good thermocompression bonding technique on beam lead devices.

Most diodes and transistors are available as chips. The back contact is soldered to the circuit and the top contact is connected to the circuit with a wire or mesh. Figure 2 shows a corner of a chip with the detail of the die attach visible. The continuous fillet around the edge is evidence of a good die attach operation. The fillet is broken by the void at the corner. Inspection specifications will limit the number and size of such voids. Most specs would permit a small void like this.

Figure 3 shows several wire bonds on a GaAs FET chip (HFET-5001). The leads are crushed by the bonding tool to about half the wire diameter. The bonds are positioned away from the pad edges. These are good examples of wire bonding.

Both chips and beam leads require special equipment and skills for assembly. In an earlier section of the catalog, beam lead Schottkies were offered as an assembly on carriers such as the H-2 outline. Special equipment is not required for these devices. Similarly, many diode chips are offered as assemblies on mini-strip and LID carriers. They are convenient for hybrid integrated circuits, but the added carrier parasitics limit the bandwidth capabilities of these devices.

Beam Lead Schottkies

Single beam lead diodes are tested for mixer performance at 9.375 GHz and at 16 GHz. Two barrier levels are available and all models are available in matched groups of 20 or more.

DC tested units are provided with maximum capacitance of 0.10, 0.15, or 0.25 pF. Two barrier levels and batch matching are also provided.

These diodes make excellent detectors as well as mixers. The low barrier units do not require DC bias.

Monolithic ring quads are also available with four capacitance ratings and two barrier levels for each capacitance rating. These quads are mainly used in double balanced mixers.

Beam Lead PIN's

Two basic beam lead PIN designs are available. Outlines 06 and 21 provide low capacitance for series designs. Outline 07 provides low resistance for shunt designs.

Chips, Ministrips, and LID's

Most diode products are available as chips, mini-strips, and LIDs. These are shown in this section of the catalog. These models are kept in stock.

Transistors

Both bipolar and GaAs FET transistors are available in chip form. Die attach and bonding procedures are shown in Application Note 974, Die Attach and Bonding Techniques for Diodes & Transistors.

The use of hybrid integrated circuits will continue to grow. Lower parasitics improve bandwidth. Small size allows miniaturization of circuits. Uniformity allows the use of automatic handling and assembly to reduce costs and improve reliability.

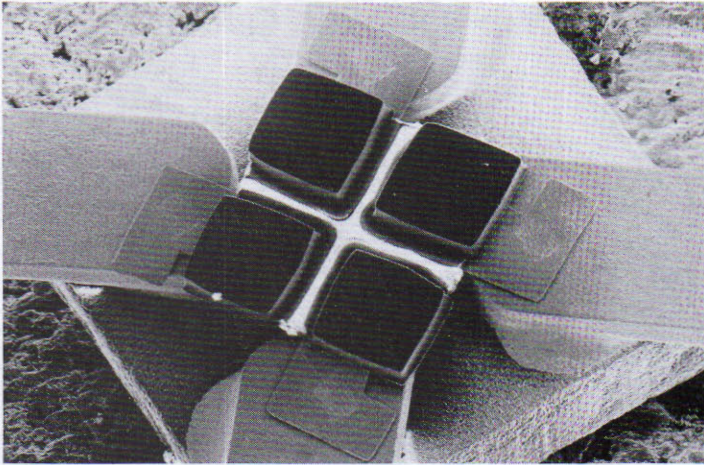


Figure 1. A beam lead diode quad bonded to a carrier.

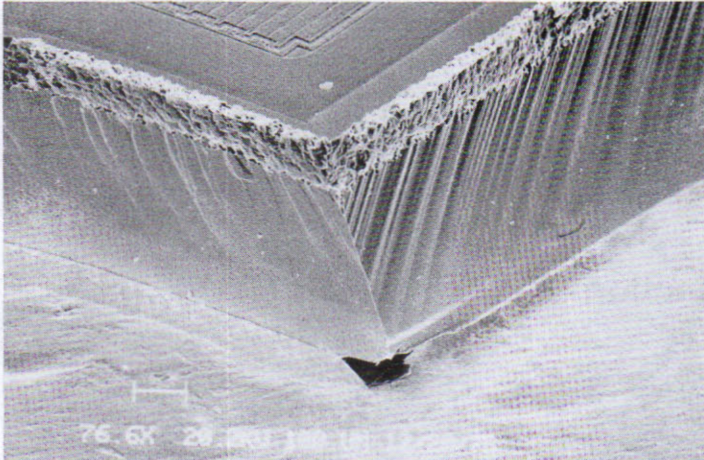


Figure 2. Chip die attach detail.

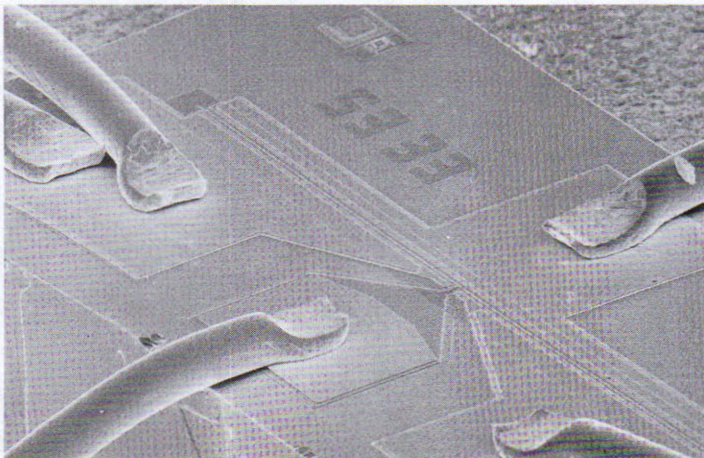


Figure 3. Wire bonds on a GaAs FET chip.

GaAs Field Effect Transistor Chip Selection Guide

Features	Typical Performance at 10 GHz	Part Number HFET-	Page Number
Low Noise Figure High Association Gain High Output Power (P_{1dB})	3.2 dB 6.9 dB 15.4 dBm	1001	167
High Linear Power High Associated 1 dB Compression Gain	19.5 dBm 6.5 dB	5001	174

Silicon Bipolar Transistor Chip Selection Guide

The line of four silicon bipolar transistor chips covers the majority of bipolar amplifier applications. The following table lists the transistor part numbers with their performance features.

Features	Typical Performance at 4 GHz	Part Number HXTR-	Page Number
Low Noise Figure High Associated Gain	2.7 dB 9.0 dB	6001	187
High Maximum Available Gain High Output Power (P_{1dB}) Low Noise Figure	11.5 dB 18.5 dBm 3.8 dB	2001	177
High Maximum Stable Gain High Output Power (P_{1dB}) Low Noise Figure	23.0 dB (at 1 GHz) 21.0 dBm 1.5 dB	3001	179
High Output Power (P_{1dB}) High Gain (at P_{1dB})	22.0 dBm (at 1 GHz) 18.0 dB	3002	181
High Output Power (P_{1dB}) High Gain (at P_{1dB})	22 dBm 8.0 dB	5001	183
High Output Power (P_{1dB}) High Gain (at P_{1dB})	27.5 dBm 7.5 dB	5002	185

Beam Lead Diode Selection Guide

SINGLE MICROWAVE SCHOTTKY DIODES (page 190)

Recommended Frequency Limit	Barrier	D.C. Specified 5082-	R.F. Specified
12.4 GHz	Low	2229	
	Medium	2709	5082-2768
18 GHz	Low	2299	
	Medium	2716	5082-2769
100 GHz	Low	2264	—
	Medium	2767	—

MICROWAVE SCHOTTKY QUADS (page 195)

	Recommended Frequency	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
Part No. 5082-	Low Barrier	9697	9697	9395	9397	9399
	Medium Barrier	9696	9696	9394	9396	9398

MICROWAVE PIN DIODES

Series Resistance	Capacitance	Part Number	Page Number
1.3Ω at 10 mA	0.12 pF at 10V	HPND-4050	201
1.8Ω at 10 mA	0.07 pF at 30V	HPND-4001	201
4.7Ω at 20 mA	.017 pF at 10V	HPND-4005	203
6.8Ω at 50 mA	0.02 pF at 0V	5082-3900	199

HEWLETT PACKARD

GENERAL PURPOSE MICROWAVE GaAs FET CHIP

HFET-1001

Features

HIGH GAIN
13.3 dB Typical Gain at 8 GHz
11.5 dB Typical at 10 GHz

LOW NOISE FIGURE
1.5 dB Typical at 4 GHz
3.2 dB Typical at 10 GHz

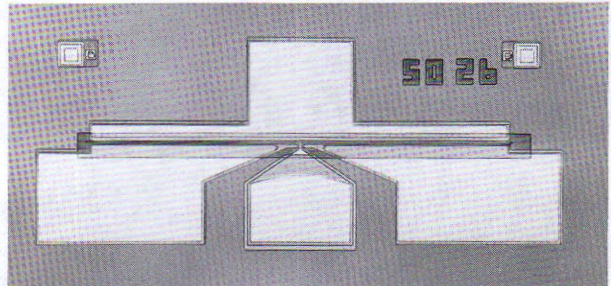
HIGH P_{1dB} LINEAR POWER
17.1 dBm Typical at 4 GHz
15.4 dBm Typical at 10 GHz

RUGGED CHIP

INTEGRAL CHANNEL PARTICLE AND SCRATCH PROTECTION

SUITABLE FOR BROADBAND APPLICATIONS

LARGE GOLD BONDING PADS



Chip Dimensions in mm (in.)
0.69 (0.027) x 0.31 (0.012) x 0.13 (0.005)
(See page 176 for bonding pad dimensions)

Description/Applications

The HFET-1001 is a gallium arsenide Schottky barrier field effect transistor chip designed for use in broadband and narrow-band applications to 12 GHz. Its rugged construction and excellent microwave performance in gain, noise figure and output power commend it for use in demanding applications such as ECM, radar and land and satellite communications.

The chip is provided with a dielectric particle and scratch protection layer over the active area. The gate width is 500 micrometers, which results in a typical linear output power of greater than 30 mW at 10 GHz and facilitates matching as low as 1.5 GHz.

Hybrid Integrated Circuits

Electrical Specifications at T_A=25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current V_{DS} = 4.0 V, V_{GS} = 0 V		mA	40		120
V_{GSP}	Pinch Off Voltage V_{DS} = 4.0 V, I_{DS} < 100 μA		V	-1.5		-5.0
g_m	Transconductance V_{DS} = 4.0V, Δ V_{GS} = 0 V to -0.5 V		mmho	30	45	
$G_{a(max)}$	Maximum Available Gain V_{DS} = 4.0 V, V_{GS} = 0 V	f = 8 GHz 10 GHz	dB		13.3 11.5	
F_{min}	Noise Figure	f = 4 GHz 8 GHz 10 GHz	dB		1.5 2.6 3.2	
G_a	Associated Gain At NF Bias V_{DS} = 3.5V I_{DS} = 15% I_{DSS} (Typ. 12 mA)	f = 4 GHz 8 GHz 10 GHz	dB		11.8 8.5 6.9	
P_{1dB}	Power Output at 1 dB Gain Compression	f = 4 GHz 8 GHz 10 GHz	dBm		17.1 16.3 15.4	
G_{1dB}	Associated 1 dB Compressed Gain V_{DS} = 5.0V, I_{DS} = 50% I_{DSS} Tuned for Maximum Output Power at +5 dBm Input	f = 4 GHz 8 GHz 10 GHz	dB		12.4 10.1 9.1	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-5.0\ V \le V_{GS} \le 0.0\ V$	5V
V_{GS}[2]	Gate-to-Source Voltage $5.0\ V \ge V_{DS} \ge 0.0V$	-5V
T_{CH}[3]	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3 x 10^6 hours at T_{CH} = 125°C (based on Activation Energy = 1.2 eV).
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. Θ_{JB} (Junction-to-Back Contact Thermal Resistance) = 100°C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-10\ V \le V_{GS} \le 0.0V$	11V
V_{GS}[2]	Gate to Source Voltage $10\ V \ge V_{DS} \ge 0.0\ V$	-10V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(max)}$	Maximum Storage Temperature	300°C

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum Forward Gate Current should not exceed 3 mA.

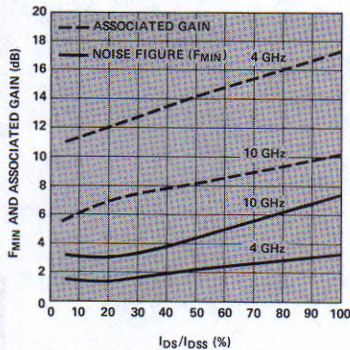


Figure 1. Typical Noise Figure and Associated Gain vs. I_{DS} as a percentage of I_{DSS} at 4 GHz and 10 GHz, V_{DS} = 3.5 V.

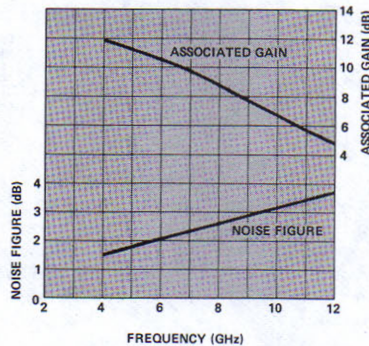


Figure 2. Typical Noise Figure and Associated Gain vs. Frequency. V_{DS} = 3.5 V, I_{DS} = 15% I_{DSS}.

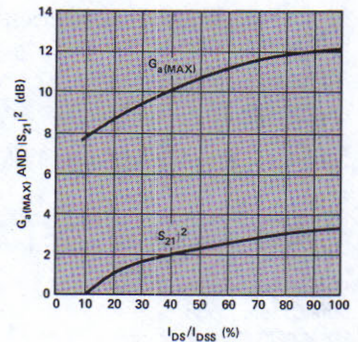


Figure 3. Typical $G_{a(max)}$ and $|S_{21}|^2$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 10 GHz, V_{DS} = 4.0 V.

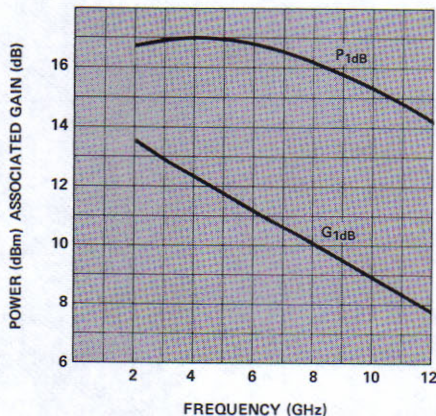


Figure 4. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Frequency at V_{DS} = 5.0 V, I_{DS} = 50% I_{DSS}.

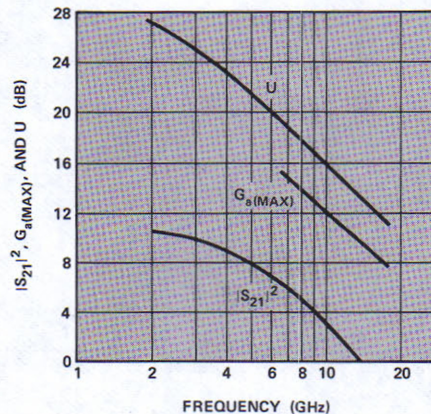


Figure 5. Mason's Gain (U), $G_{a(max)}$ and $|S_{21}|^2$ vs. Frequency, V_{DS} = 4.0 V, V_{GS} = 0.0 V.

Typical S-Parameters*

HIGH GAIN BIAS V_{DS} = 4.0V, V_{GS} = 0V.

Freq. (GHz)	S11		S21			S12			S22	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.94	-41	10.52	3.36	148	-34.42	0.02	71	0.79	-9
3.0	0.90	-62	10.04	3.18	133	-31.06	0.03	62	0.76	-17
4.0	0.85	-80	8.95	2.80	120	-30.17	0.03	57	0.76	-19
5.0	0.82	-96	7.96	2.50	107	-29.90	0.03	53	0.74	-24
6.0	0.80	-106	6.88	2.21	97	-29.37	0.03	50	0.74	-29
7.0	0.78	-117	6.24	2.05	89	-29.12	0.04	50	0.74	-33
8.0	0.77	-125	5.06	1.79	80	-30.17	0.04	49	0.74	-40
9.0	0.76	-132	4.08	1.60	72	-28.87	0.04	52	0.76	-44
10.0	0.76	-135	3.03	1.42	66	-28.87	0.04	55	0.76	-50
11.0	0.74	-139	2.61	1.35	62	-28.64	0.04	60	0.78	-52
12.0	0.73	-141	1.52	1.19	57	-28.40	0.04	64	0.79	-54

LINEAR POWER BIAS V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}

Freq. (GHz)	S11		S21			S12			S22	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.93	-43	8.69	2.72	146	-33.12	0.02	69	0.77	-9
3.0	0.90	-62	7.96	2.50	131	-30.46	0.03	61	0.76	-13
4.0	0.86	-80	7.08	2.26	119	-29.07	0.04	55	0.74	-17
5.0	0.82	-94	6.20	2.04	106	-28.04	0.04	51	0.73	-21
6.0	0.77	-106	5.05	1.79	96	-27.52	0.04	47	0.72	-26
7.0	0.76	-115	4.11	1.61	88	-27.19	0.04	45	0.72	-30
8.0	0.75	-123	3.42	1.48	81	-26.98	0.05	47	0.72	-33
9.0	0.74	-128	2.61	1.35	72	-26.75	0.05	46	0.73	-38
10.0	0.72	-132	1.65	1.21	65	-26.57	0.05	48	0.73	-42
11.0	0.71	-138	1.03	1.13	61	-26.36	0.05	50	0.74	-46
12.0	0.71	-142	0.68	1.08	54	-25.89	0.05	52	0.75	-50

MINIMUM NOISE FIGURE BIAS V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

Freq. (GHz)	S11		S21			S12			S22	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	MAg.	Ang.
2.0	0.95	-32	6.73	2.17	152	-28.64	0.04	72	0.72	-11
3.0	0.91	-49	6.44	2.10	139	-25.35	0.05	63	0.74	-18
4.0	0.86	-66	5.83	1.96	124	-23.48	0.07	55	0.74	-23
5.0	0.82	-81	5.20	1.82	111	-22.50	0.08	48	0.71	-28
6.0	0.79	-94	4.13	1.61	99	-22.16	0.08	42	0.70	-34
7.0	0.76	-104	3.67	1.53	91	-21.83	0.08	38	0.69	-40
8.0	0.75	-113	2.61	1.35	80	-21.41	0.09	33	0.69	-47
9.0	0.74	-120	1.66	1.21	71	-21.51	0.08	30	0.70	-54
10.0	0.74	-125	0.68	1.08	65	-21.72	0.08	30	0.71	-58
11.0	0.72	-128	0.10	1.01	60	-21.72	0.08	31	0.72	-60
12.0	0.71	-131	-0.85	0.91	55	-21.83	0.08	31	0.74	-62

*S-parameters are measured and referenced directly to the chip terminals (bonding pads). Specific parasitics due to bonding wires and die attachment must be considered in the user's individual circuit designs.

HEWLETT PACKARD

LOW NOISE MICROWAVE GaAs FET CHIP

HFET-2001

Features

LOW NOISE FIGURE
- **1.9 dB Typical at 8 GHz**
- **2.7 dB Typical at 12 GHz**

HIGH ASSOCIATED GAIN
- **10.3 dB Typical at 8 GHz**
- **8.1 dB Typical at 12 GHz**

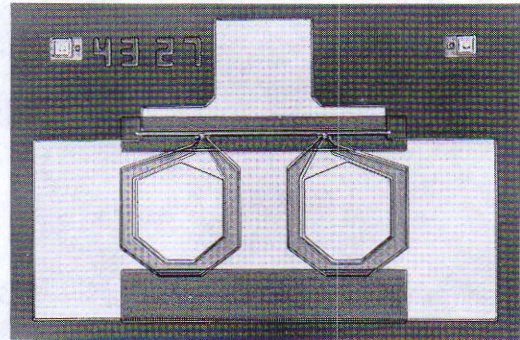
HIGH OUTPUT POWER
- **+14.2 dBm Linear Power at 12 GHz**

CHARACTERIZED TO 18 GHz

RUGGED CHIP

INTEGRAL CHANNEL PARTICLE AND SCRATCH PROTECTION

LARGE GOLD BONDING PADS



Chip Dimensions in mm (in.)
0.55 (0.022) x 0.39 (0.015) x 0.13 (0.005)
(See page 4 for bonding pad dimensions.)

Description/Applications

The HFET-2001 is a gallium arsenide Schottky gate field effect transistor designed for consistent broadband or narrow-band operation over the frequency range of 2 GHz to 18 GHz. Excellent noise and gain performance coupled with wide dynamic range capability make this device ideally suited for such applications as ECM, wideband surveillance and warning systems.

In addition, these characteristics lend themselves to ease of circuit design in applications such as radar and communications equipment.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameter and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 3.5V$, $V_{GS} = 0V$		mA	25	45	90
V_{GSP}	Pinch Off Voltage, $V_{DS} = 3.5V$, $I_{DS} < 500\ \mu A$		V	-0.5	-2.0	-4.0
gm	Transconductance, $V_{DS} = 3.5V$, $\Delta V_{GS} = 0V$ to $-0.5V$		mmho	20	32	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 4.0V$, $I_{DS} = 75\%\ I_{DSS}$	f = 12 GHz 18 GHz	dB		11.5 9.0	
F_{MIN}	Minimum Noise Figure	f = 4 GHz 8 GHz 12 GHz 18 GHz	dB		1.2 1.9 2.7 3.4	
G_a	Associated Gain at N.F. Minimum Bias $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$[1]	f = 4 GHz 8 GHz 12 GHz 18 GHz	dB		14.5 10.3 8.1 5.9	
P_{1dB}	Power Output at 1 dB Gain Compression	f = 8 GHz 12 GHz	dBm		+14.6 +14.2	
G_{1dB}	Associated 1 dB Compressed Gain $V_{DS} = 4.0V$, $I_{DS} = 50\%\ I_{DSS}$ Tuned for Maximum Output at +3 dBm Input	f = 8 GHz 12 GHz	dB		11.5 8.9	

Note 1. Devices are biased at 15% I_{DSS} or 6 mA, whichever is greater.

Recommended Maximun Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-4V \le V_{GS} \le 0V$	4V
V_{GS}[2]	Gate to Source Voltage $4V \ge V_{DS} \ge 0V$	-4V
T_{CH}[3]	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3 x 10^6 hours at T_{CH} = 125°C (based on Activation Energy = 1.1 eV).
2. Maximum continuous forward gate current should not exceed 1.5 mA.
3. Θ_{JB} (Junction-to-Back Contact Thermal Resistance) = 180°C/W.

Absolute Maximum Ratings

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-4V \le V_{GS} \le 0V$	10V
V_{GS}[2]	Gate to Source Voltage $4V \ge V_{DS} \ge 0V$	-6V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(max)}$	Maximum Storage Temperature	250°C

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward gate current should not exceed 2 mA.
3. See Handling and Use Precautions (pg. 173)

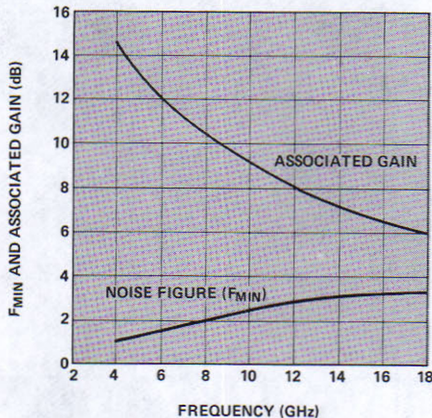


Figure 1. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency, V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}[1].

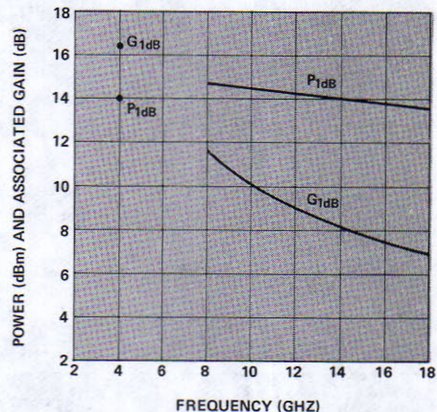


Figure 2. Typical Output Power at 1 dB Compression and Associated 1 dB Compressed Gain vs. Frequency. V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}. (Tuned for Maximum Output Power at +3 dBm Input Power, 4 GHz Data at 0 dBm Input Power)

Typical Noise Parameters

Freq. (GHz)	Γ_o Mag.	Γ_o Ang.	F_{MIN} (dB)	R_N (ohms)
4	.74	38	1.2	56
8	.62	74	1.9	43
12	.60	86	2.7	40
18	.54	122	3.4	25

Optimum Input Reflection Coefficient (Γ_o). Associated Noise Figure, (F_{MIN}), and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}[1].

Note 1:
Devices are biased at 15% I_{DSS} or 6 mA, whichever is greater.

Typical S-Parameters*

HIGH GAIN BIAS V_{DS} = 4.0V, I_{DS} = 75% I_{DSS}

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.5	0.99	-7	8.05	2.53	174	-46.02	0.01	86	0.76	-3
1.0	0.99	-14	7.89	2.48	168	-40.00	0.01	83	0.76	-5
2.0	0.97	-27	7.57	2.39	159	-34.42	0.02	77	0.75	-9
4.0	0.93	-48	6.81	2.19	140	-29.37	0.03	68	0.75	-15
6.0	0.88	-68	6.13	2.03	124	-26.94	0.05	61	0.73	-21
8.0	0.82	-87	5.25	1.83	108	-26.02	0.05	56	0.70	-28
10.0	0.79	-104	4.32	1.65	94	-25.85	0.05	55	0.69	-36
12.0	0.76	-117	3.42	1.48	83	-26.02	0.05	58	0.69	-41
14.0	0.74	-130	2.90	1.40	71	-25.51	0.05	64	0.67	-46
16.0	0.72	-145	2.35	1.31	60	-24.44	0.06	66	0.66	-54
18.0	0.72	-158	1.59	1.20	48	-23.88	0.06	68	0.66	-63

LINEAR POWER BIAS V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.5	0.99	-7	7.80	2.45	174	-44.44	0.01	87	0.74	-3
1.0	0.99	-14	7.65	2.41	168	-38.42	0.01	82	0.74	-6
2.0	0.97	-26	7.34	2.33	159	-33.15	0.02	77	0.74	-9
4.0	0.93	-46	6.62	2.14	141	-27.96	0.04	67	0.73	-16
6.0	0.88	-65	5.99	2.00	125	-25.68	0.05	60	0.71	-22
8.0	0.83	-85	5.16	1.81	109	-24.58	0.06	53	0.68	-30
10.0	0.79	-101	4.28	1.64	95	-24.29	0.06	51	0.66	-37
12.0	0.76	-113	3.40	1.48	84	-24.44	0.06	52	0.66	-43
14.0	0.73	-126	2.85	1.39	73	-24.01	0.06	54	0.64	-48
16.0	0.71	-141	2.39	1.32	61	-23.22	0.07	55	0.63	-56
18.0	0.71	-154	1.66	1.21	49	-22.97	0.07	56	0.62	-65

MINIMUM NOISE FIGURE BIAS V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}[1]

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.5	0.98	-6	5.78	1.95	174	-41.94	0.01	86	0.76	-3
1.0	0.99	-12	5.64	1.91	169	-36.48	0.02	82	0.75	-6
2.0	0.97	-23	5.36	1.85	160	-30.75	0.03	77	0.75	-10
4.0	0.94	-42	4.77	1.73	142	-25.51	0.05	66	0.74	-17
6.0	0.89	-60	4.28	1.64	127	-22.85	0.07	57	0.71	-24
8.0	0.84	-78	3.61	1.52	111	-21.51	0.08	48	0.68	-32
10.0	0.80	-94	2.85	1.39	97	-21.01	0.09	43	0.66	-40
12.0	0.77	-106	2.07	1.27	85	-21.11	0.09	39	0.65	-46
14.0	0.74	-119	1.62	1.21	74	-20.92	0.09	38	0.63	-52
16.0	0.72	-133	1.26	1.16	62	-20.45	0.09	34	0.61	-60
18.0	0.71	-147	0.59	1.07	49	-20.72	0.09	31	0.60	-70

*S-Parameters and Γ values are measured in a microstrip chip test fixture which includes bond wire parasitics. Refer to H.P. Application Bulletin No. AB37 for details.

Handling And Use Precautions

1. Device voltage breakdown and permanent damage can be caused by the following:

   a. Inductive pickup from large transformers, switching power supplies, induction ovens, etc. Use shielded signal and power cables.

   b. Transients from voltmeters, multimeters, signal generators, curve tracers, etc. Avoid turning instrument power on and off, or switching between instrument ranges when bias is applied to the device.

      For thermocompression and pulse bonders, insure that bonders are adequately grounded.

   c. Static Discharge—Assembly and test personnel, as well as tweezers or any other pick-up tool, should be grounded to the test or assembly station, preventing the build-up of static charge which can damage the gate area if the charge is allowed to pass through it. During the mounting procedure, insure assembly equipment is adequately grounded.

      Static discharge during handling, testing, assembly, and final seal can induce increased reverse gate leakage of a resistive nature.

2. Light Sensitivity — GaAs FETs characteristically are light sensitive and this should be borne in mind when making DC and RF measurements. Ensure that the measurement environment is the same as the use environment.

3. Moisture—The presence of excessive moisture on a FET chip surface under normal operating voltages may cause irreversible damage.

4. Application of Bias—When applying bias to the FET, first apply the gate voltage, then the drain voltage. When removing bias, remove the gate voltage last.

Die Attaching

The FET chip can be die attached manually using a pair of tweezers, or automatically using a collet. In either case, provide a flow of nitrogen over the stage area. Start with a stage temperature of 300° C and raise as required. The chip should not be exposed, however, to greater than 320° C for more than 30 seconds. A 80/20 gold/tin preform of 625 x 250 x 25 micrometers (.025 x .010 x .001 in.) or standard round preform of equivalent volume is recommended. When using tweezers make sure that the chip is level to facilitate subsequent capillary wire bonding. The requirement is less critical for wedge bonding.

Gallium arsenide material is more brittle than silicon and should be handled with care. When using a collet, it is important to have a flat die attach surface. By using a minimum of downward force, the chance of breaking the chip is reduced.

Wire Bonding

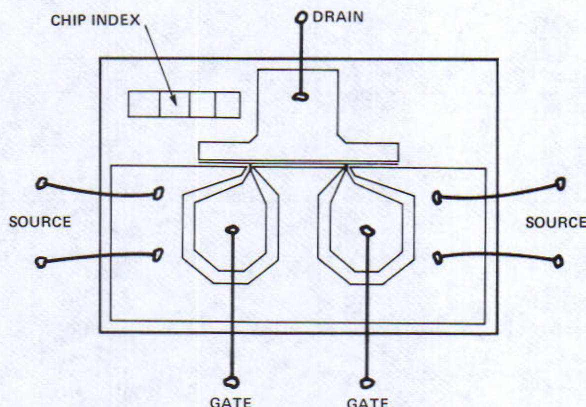
Either thermal-compression or ultrasonic wire bonding of 18/25 micrometer (.0007"/.001") diameter, pure gold, stress relieved wire can be used.

For thermal-compression bonding, start with a stage temperature of 225°C and a tip temperature of 150°C. The typical bonding force should be approximately 30 grams and should not exceed 40 grams.

For ultrasonic bonding, the stage can be heated to 150°C with a bonding force of approximately 25 grams. Scrubbing frequency, amplitude and time is bonder dependent and is determined empirically.

The wire bond on the gate pad should remain well inside the pad boundaries. Additionally, mechanical contact with the transparent channel areas must be avoided to prevent gate damage.

Hybrid Integrated Circuits



BONDING PAD DIMENSIONS mm (in.)

SOURCE	0.19 x 0.09 (.007 x .0035)
DRAIN	0.10 x 0.10 (.0039 x .0039)
GATE	0.09 x 0.08 (.0035 x .0031)

Figure 3. Bonding Diagram and Pad Dimensions.

HEWLETT PACKARD

MICROWAVE GaAs FET CHIP

HFET-5001

Features

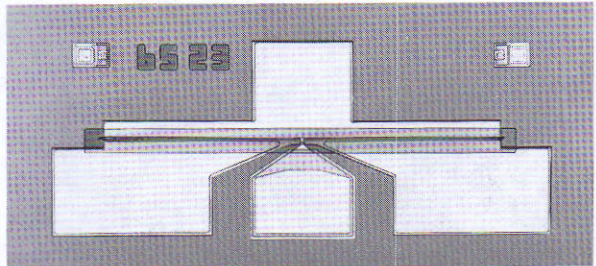
HIGH P_{1dB} LINEAR POWER
18.5 dBm Typical at 12 GHz
19.5 dBm Typical at 10 GHz
21.0 dBm Typical at 4 GHz with 11.0 dB Associated Gain

SUITABLE FOR BROADBAND APPLICATIONS

RUGGED CHIP

INTEGRAL CHANNEL PARTICLE AND SCRATCH PROTECTION

LARGE GOLD BONDING PADS



Chip Dimensions in mm (in.)
0.69 (0.027) x 0.31 (0.012) x 0.13 (0.005)
(See page 212 for bonding pad dimensions.)

Description

The HFET-5001 is a gallium arsenide Schottky barrier field effect transistor chip designed for high gain and linear power from 2 to 14 GHz. The chip is provided with a dielectric particle and scratch protection layer over the active area. The gate width is 500 micrometers resulting in a typical linear output power of greater than 100 mW at 8 GHz.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current $V_{DS} = 4.0V$, $V_{GS} = 0V$	mA	80		170
V_{GSP}	Pinch Off Voltage $V_{DS} = 3.0$ V, $I_{DS} < 1$ mA	V	−1.5		−8.0
g_m	Transconductance $V_{DS} = 4.0V$, $\Delta V_{GS} = 0V$ to $-0.5V$	mmho	25	30	
P_{1dB}	Power Output at 1 dB Gain Compression Tuning Fixed for Maximum Power Output at: $P_{IN} = +10$ dBm f = 4 GHz $P_{IN} = +12$ dBm f = 8 GHz 10 GHz 12 GHz	dBm		21.0 20.5 19.5 18.5	
G_{1dB}	Associated 1dB Compressed Gain f = 4 GHz 8 GHz 10 GHz 12 GHz Conditions for above: $V_{DS} = 5.0V$, $I_{DS} = 50\%$ I_{DSS}	dB		11.0 8.0 6.5 5.5	

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage -8.0V ≤ V_{GS} ≤ 0.0V	5V
V_{GS} [2]	Gate To Source Voltage 5.0V ≥ V_{DS} ≥ 0.0V	-8V
T_{CH} [3]	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) of 1.3 x 10^6 hours at T_{CH} = 125°C (based on Activation Energy = 1.2 eV).
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. θ_{JB} (Junction-to-Back Contact Thermal Resistance) = 100°C/W.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage -10V ≤ V_{GS} ≤ 0V	10V
V_{GS} [2]	Gate To Source Voltage 10V ≥ V_{DS} ≥ 0V	-10V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	300°C

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum Forward Gate Current should not exceed 3 mA.

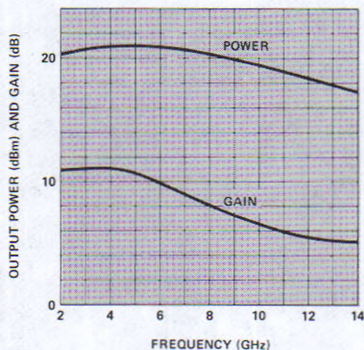


Figure 1. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Frequency at V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

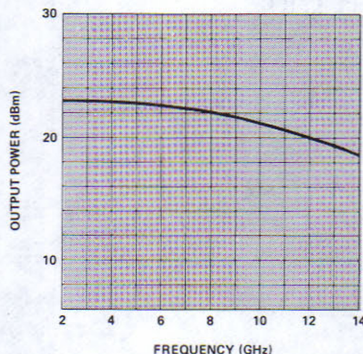


Figure 2. Typical Output Power at 3 dB Gain vs. Frequency, V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

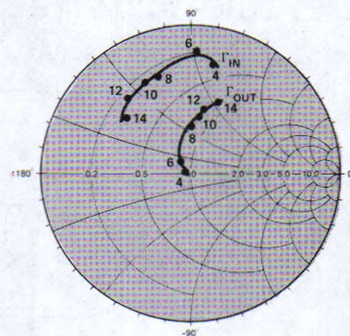


Figure 3. Typical Source (Γ_{IN}) and Load (Γ_{OUT}) Impedance for Maximum P_{1dB} Output Power (tuned with P_{IN} = +12 dBm) in the 4 to 14 GHz frequency range, V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

Hybrid Integrated Circuits

Typical Small Signal S-Parameters V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}

Freq. (GHz)	S11		S21			S12			S22	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.00	.97	− 32	7.72	2.43	153	−34.00	0.02	74	0.69	−10
3.00	.95	− 47	7.22	2.30	141	−30.46	0.03	67	0.68	−14
4.00	.91	− 61	6.84	2.20	130	−27.96	0.04	62	0.67	−19
5.00	.87	− 76	6.09	2.02	118	−26.02	0.05	55	0.67	−23
6.00	.84	− 87	5.37	1.86	109	−26.02	0.05	51	0.66	−28
7.00	.82	− 96	4.66	1.71	100	−26.02	0.05	49	0.65	−33
8.00	.81	−106	3.92	1.57	92	−24.44	0.06	47	0.65	−36
9.00	.78	−115	3.03	1.42	84	−24.44	0.06	45	0.66	−42
10.00	.77	−119	2.28	1.30	79	−24.44	0.06	46	0.66	−44
11.00	.77	−122	2.01	1.26	74	−24.44	0.06	48	0.66	−49
12.00	.76	−124	1.30	1.16	65	−24.44	0.06	48	0.67	−53
13.00	.75	−126	0.75	1.09	62	−24.44	0.06	49	0.69	−57
14.00	.75	−128	0.04	1.01	58	−23.10	0.07	53	0.70	−62

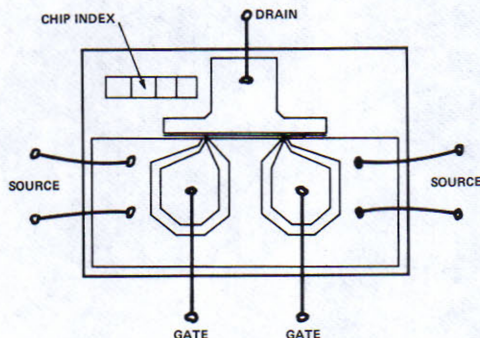
Handling And Use Precautions

1. Device voltage breakdown and permanent damage can be caused by the following:
   a. Inductive pickup from large transformers, switching power supplies, induction ovens, etc. Use shielded signal and power cables.
   b. Transients from voltmeters, multimeters, signal generators, curve tracers, etc. Avoid turning instrument power on and off, or switching between instrument ranges when bias is applied to the device.

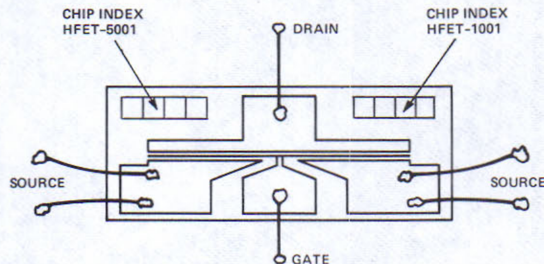
      For thermocompression and pulse bonders, insure that bonders are adequately grounded.
   c. Static Discharge—Assembly and test personnel, as well as tweezers or any other pick-up tool, should be grounded to the test or assembly station, preventing the build-up of static charge which can damage the gate area if the charge is allowed to pass through it. During the mounting procedure, insure assembly equipment is adequately grounded.

      Static discharge during handling, testing, assembly, and final seal can induce increased reverse gate leakage of a resistive nature.
2. Light Sensitivity — GaAs FETs characteristically are light sensitive and this should be borne in mind when making DC and RF measurements. Ensure that the measurement environment is the same as the use environment.
3. Moisture—The presence of excessive moisture on a FET chip surface under normal operating voltages may cause irreversible damage.
4. Application of Bias—When applying bias to the FET, first apply the gate voltage, then the drain voltage. When removing bias, remove the gate voltage last.

Die Attach And Wire Bonding



Bonding Diagram and Pad Dimensions for HFET-2001.



Bonding Diagram and Pad Dimensions for HFET-1001, HFET-5001.

Die Attaching

The FET chip can be die attached manually using a pair of tweezers, or automatically using a collet. In either case, provide a flow of nitrogen over the stage area. Start with a stage temperature of 300°C and raise as required. The chip should not be exposed, however, to greater than 320°C for more than 30 seconds. A 80/20 gold/tin preform of 625 x 250 x 25 micrometers (.025 x .010 x .001 in.) or standard round preform of equivalent volume is recommended. When using tweezers make sure that the chip is level to facilitate subsequent capillary wire bonding. The requirement is less critical for wedge bonding.

Gallium arsenide material is more brittle than silicon and should be handled with care. When using a collet, it is important to have a flat die attach surface. By using a minimum of downward force, the chance of breaking the chip is reduced.

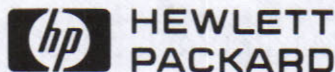
Wire Bonding

Either thermal-compression or ultrasonic wire bonding of 18/25 micrometer (.0007"/.001") diameter, pure gold, stress relieved wire can be used.

For thermal-compression bonding, start with a stage temperature of 225°C and a tip temperature of 150°C. The typical bonding force should be approximately 30 grams and should not exceed 40 grams.

For ultrasonic bonding, the stage can be heated to 150°C with a bonding force of approximately 25 grams. Scrubbing frequency, amplitude and time is bonder dependent and is determined empirically.

The wire bond on the gate pad should remain well inside the pad boundaries. Additionally, mechanical contact with the transparent channel areas must be avoided to prevent gate damage.



GENERAL PURPOSE TRANSISTOR CHIP

HXTR-2001

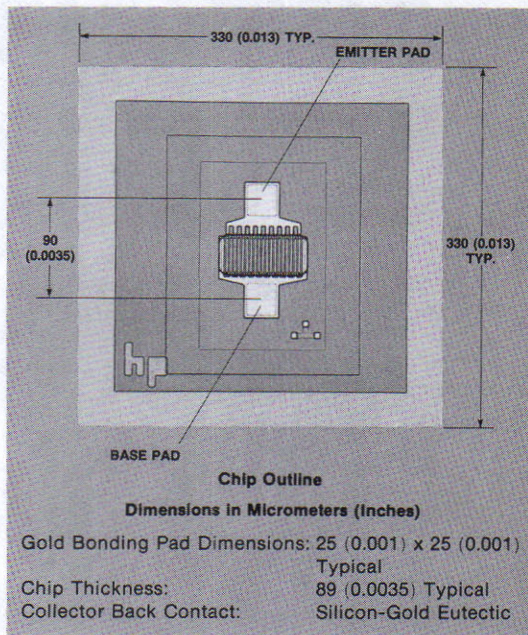
Features

HIGH GAIN
17.5 dB Typical at 2 GHz

HIGH OUTPUT POWER
20.0 dBm P_{1dB} Typical at 2 GHz

LOW NOISE FIGURE
3.8 dB Typical at 4 GHz

WIDE DYNAMIC RANGE



Chip Outline

Dimensions in Micrometers (Inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Description/Applications

The HXTR-2001 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustment. The HXTR-2001 features a Ti/Pt/Au metallization system and a dielectric scratch protection over its active area to insure reliable operation.

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at I_C=100μA		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at V_{CE}=15V		3041.1**	nA			500
I_{CBO}	Collector Cutoff Current at V_{CB}=15V		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=15V, I_C=15mA		3076.1*	—	50	120	220
$G_{a(max)}$	Maximum Available Gain	f=2GHz		dB		17.5	
		4GHz				11.5	
P_{1dB}	Power Output at 1dB Gain Compression	f=2GHz		dBm		20.0	
	Conditions for above: V_{CE} = 15V, I_C = 25 mA, Θ_{JA} = 210° C/W	4GHz				18.5	
F_{MIN}	Minimum Noise Figure	f=1.5GHz	3246.1	dB		2.2	
	Conditions for above: V_{CE} = 15V, I_C = 15 mA, Θ_{JA} = 210° C/W	4GHz				3.8	

*300μs wide pulse measurement <2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	35 mA
P_T	Total Device Dissipation[2]	450 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in Median Time To Failure (MTTF) to below the design goal of 1×10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a θ_{JB} (Junction-to-Back contact thermal resistance) of 125°C/W.
   Total θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	300°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

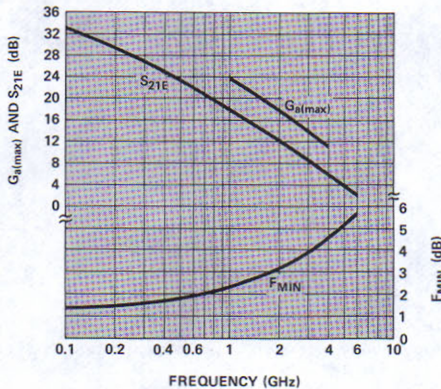


Figure 1. Typical $G_{a(max)}$, S_{21E}, and Noise Figure (F_{MIN}) vs. Frequency at V_{CE} = 15V, I_C = 25mA.

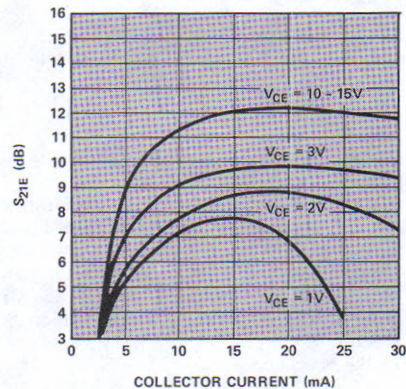
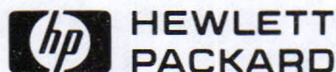


Figure 2. Typical S_{21E} vs. Current at 2GHz.

Typical S-Parameters* V_{CE} = 15V, I_C = 25mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.57	-88	33.3	46.2	144	-42	0.008	58	0.85	-20
200	0.68	-124	30.2	32.5	123	-39	0.011	43	0.67	-26
300	0.72	-141	27.6	23.9	113	-38	0.013	37	0.56	-26
400	0.74	-150	25.4	18.7	106	-37	0.014	35	0.51	-24
500	0.75	-156	23.7	15.3	102	-37	0.014	35	0.48	-22
600	0.76	-160	22.2	12.9	99	-36	0.015	36	0.46	-21
700	0.76	-163	20.8	11.0	97	-36	0.015	37	0.45	-20
800	0.76	-165	19.9	9.8	95	-36	0.016	38	0.44	-19
900	0.76	-167	18.8	8.7	93	-36	0.016	40	0.44	-18
1000	0.76	-168	18.0	7.9	91	-35	0.017	42	0.44	-18
1500	0.77	-172	14.5	5.3	85	-34	0.021	49	0.43	-18
2000	0.77	-175	12.0	4.0	81	-32	0.025	54	0.43	-20
2500	0.77	-176	10.1	3.2	77	-31	0.029	58	0.43	-23
3000	0.77	-177	8.6	2.7	73	-29	0.034	60	0.43	-26
3500	0.77	-178	7.2	2.3	69	-28	0.038	61	0.44	-29
4000	0.76	-179	6.0	2.0	66	-27	0.043	62	0.44	-32
4500	0.76	-179	5.1	1.8	63	-26	0.048	62	0.45	-35
5000	0.76	-179	4.1	1.6	59	-26	0.052	62	0.45	-38
5500	0.76	-180	3.5	1.5	56	-25	0.057	62	0.46	-41
6000	0.76	-180	2.9	1.4	53	-24	0.062	61	0.47	-44

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.



GENERAL PURPOSE TRANSISTOR CHIP

HXTR-3001

Features

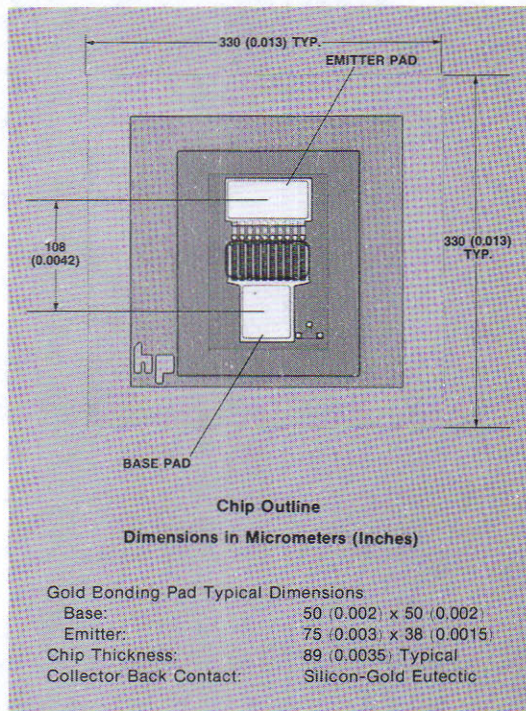
HIGH GAIN
16 dB Typical at 2 GHz

HIGH OUTPUT POWER
21.0 dBm P_{1dB} Typical at 1 GHz

LOW NOISE FIGURE
1.2 dB Typical at 500 MHz

WIDE DYNAMIC RANGE

LARGE GOLD BONDING PADS



Chip Outline

Dimensions in Micrometers (Inches)

Gold Bonding Pad Typical Dimensions
- Base: 50 (0.002) x 50 (0.002)
- Emitter: 75 (0.003) x 38 (0.0015)

Chip Thickness: 89 (0.0035) Typical
Collector Back Contact: Silicon-Gold Eutectic

Description/Applications

The HXTR-3001 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustment. The HXTR-3001 features a Ti/Pt/Au metallization system and a dielectric scratch protection over its active area to insure reliable operation. Its large gold bonding pads facilitate use of 25 μm (1 mil) gold bond wires frequently used in hybrid applications.

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$		3041.1**	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$		3076.1*	—	50	120	220
$G_{a(max)}$	Maximum Available Gain Conditions: $V_{CE}=15V$, $I_C=15$ mA, $\Theta_{JA}=210°C/W$	f = 2 GHz		dB		16	
P_{1dB}	Power Output at 1 dB Gain Compression Conditions: $V_{CE}=15V$, $I_C=25$ mA, $\Theta_{JA}=210°C/W$	f = 1 GHz 2 GHz		dBm		21.0 19.0	
F_{MIN}	Minimum Noise Figure Conditions: $V_{CE}=10V$, $I_C=7$ mA, $\Theta_{JA}=210°C/W$	f = 500 MHz 1 GHz 2 GHz	3246.1	dB		1.2 1.5 2.2	

*300μs wide pulse measurement <2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions [1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	35 mA
P_T	Total Device Dissipation [2]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a θ_{JB} (Junction-to-Back contact thermal resistance) of 125°C/W.

Total θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Recommended Die Attach and Bonding Procedures

Eutectic Die Attach at a stage temperature of 410 ± 10° C under an N_2 ambient. Chip should be lightly scrubbed using a tweezer and eutectic should flow within five seconds.

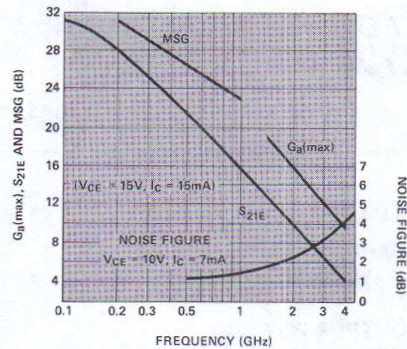


Figure 1. Typical $G_{a(max)}$, S_{21E}, Maximum Stable Gain (MSG), and Noise Figure (F_{MIN}) vs. Frequency

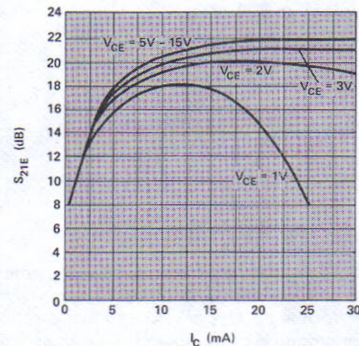


Figure 2. Typical S_{21E} vs. Current of 500 MHz

Thermocompression Wire Bond at a stage temperature of 310 ± 10° C, using a tip force of 30 ± 5 grams with 0.7 or 1.0 mil gold wire. A one mil minimum wire clearance at the passivation edge is recommended. (Ultrasonic bonding is not recommended.)

Packaging — The chip should be packaged into a clean, dry, hermetic environment.

Typical S-Parameters* V_{CE} = 15V, I_C = 15 mA

Freq. (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} (dB)	S_{21} Mag.	S_{21} Ang.	S_{12} (dB)	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.651	-74	30.6	34.037	146	-37.2	0.014	59	0.851	-23
200	0.714	-113	27.8	24.657	125	-33.9	0.020	43	0.659	-33
300	0.741	-132	25.3	18.407	114	-32.9	0.023	36	0.539	-36
400	0.754	-143	23.2	14.462	107	-32.3	0.024	33	0.471	-36
500	0.761	-151	21.5	11.835	102	-32.0	0.025	31	0.429	-35
600	0.765	-155	20.0	9.995	98	-31.7	0.026	32	0.405	-34
700	0.767	-159	18.7	8.634	95	-31.5	0.027	32	0.389	-34
800	0.768	-162	17.6	7.592	93	-31.2	0.028	33	0.377	-34
900	0.769	-164	16.6	6.773	91	-31.0	0.028	34	0.370	-34
1000	0.770	-166	15.7	6.111	89	-30.7	0.029	35	0.365	-34
1500	0.770	-171	12.2	4.096	81	-29.3	0.034	41	0.358	-38
2000	0.769	-174	9.8	3.075	74	-28.0	0.040	44	0.364	-43
2500	0.766	-176	7.8	2.459	69	-26.8	0.046	47	0.375	-49
3000	0.763	-177	6.2	2.046	63	-25.7	0.052	48	0.389	-55
3500	0.760	-178	4.9	1.750	58	-24.7	0.058	48	0.405	-61
4000	0.756	-179	3.7	1.528	53	-23.8	0.064	48	0.423	-66

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

HEWLETT PACKARD

LINEAR POWER TRANSISTOR CHIP

HXTR-3002

Features

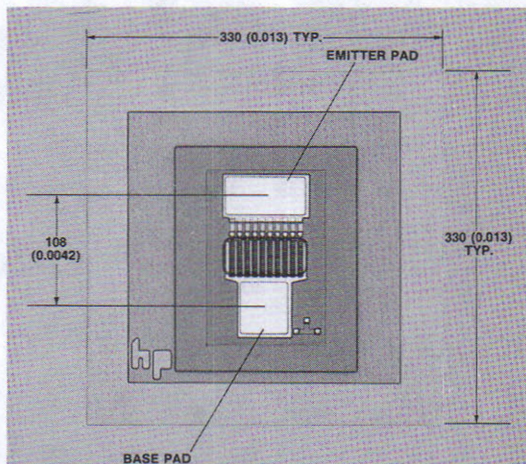
HIGH P_{1dB} LINEAR POWER
22 dBm Typical at 1 GHz

HIGH P_{1dB} GAIN
18.0 dB Typical at 1 GHz

HIGH S_{21E} GAIN
16.5 dB Typical at 500 MHz

WIDE DYNAMIC RANGE

LARGE GOLD BONDING PADS



Chip Outline
Dimensions in Micrometers (Inches)

Gold Bonding Pad Typical Dimensions

Base:	50 (0.002) x 50 (0.002)
Emitter:	75 (0.003) x 38 (0.0015)
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Description/Applications

The HXTR-3002 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustment. The HXTR-3002 features a Ti/Pt/Au metallization system, a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness. Its large gold bonding pads facilitate use of 25 μm (1 mil) gold bond wires frequently used in hybrid applications.

The superior power, gain and dynamic range performance of the HXTR-3002 commend it for RF and IF use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications.

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C = 3$ mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C = 15$ mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B = 30$ μA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB} = 2$ V		3061.1*	μA			2
I_{CES}	Collector-Emitter Leakage Current at $V_{CE} = 32$ V		3041.1**	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB} = 20$ V		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 18$ V, $I_C = 30$ mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1 dB Gain Compression	f = 1 GHz		dBm		22	
G_{1dB}	Associated 1 dB Compressed Gain	f = 1 GHz		dB		18	
S_{21E}	Transducer Gain	f = 500 MHz 1 GHz		dB		16.5 13.6	
η	Power-Added Efficiency at 1 dB Compression	f = 1 GHz		%		29	
	Test Conditions: $V_{CE} = 18$ V, $I_C = 30$ mA, $\Theta_{JA} = 210°$ C/W						

*300 μs wide pulse measurement at ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	DC Collector Current	50 mA
P_T	Total Device Dissipation[2]	700 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in Median Time To Failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 125°C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4.0V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.4W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	300°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

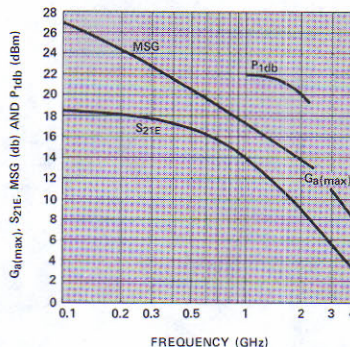


Figure 1. Typical $G_{a(max)}$, S_{21E}, Maximum Stable Gain (MSG) and Power Output at 1 dB Gain Compression (P_{1dB}) vs. Frequency, V_{CE} = 18V, I_C = 30 mA.

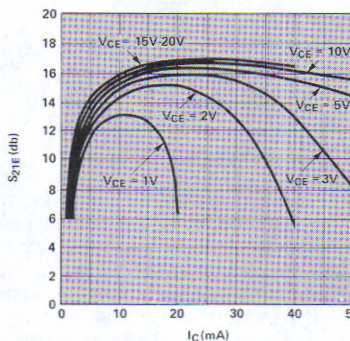


Figure 2. Typical S_{21E} vs. Current at 500 MHz

Recommended Die Attach and Bonding Procedures

Eutectic Die Attach at a stage temperature of 410 ± 10°C under an N_2 ambient. Chip should be lightly scrubbed using a tweezer and eutectic should flow within five seconds.

Thermocompression Wire Bond at a stage temperature of 310 ± 10°C, using a tip force of 30 ± 5 grams with 0.7 or 1.0 mil gold wire. A one mil minimum wire clearance at the passivation edge is recommended. (Ultrasonic bonding is not recommended.)

Packaging — The chip should be packaged into a clean, dry, hermetic environment.

Typical S-Parameters* V_{CE} = 18V, I_C = 30 mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.658	-17	18.5	8.439	170	-35.9	0.016	82	0.991	-7
200	0.656	-32	18.3	8.180	161	-30.1	0.031	75	0.965	-14
300	0.652	-47	17.8	7.792	153	-27.0	0.045	68	0.926	-20
400	0.648	-60	17.3	7.334	145	-25.0	0.056	62	0.881	-25
500	0.644	-72	16.7	6.845	138	-23.7	0.066	56	0.833	-29
600	0.641	-82	16.1	6.366	132	-22.7	0.073	52	0.787	-33
700	0.637	-91	15.4	5.911	126	-22.0	0.080	48	0.744	-36
800	0.634	-99	14.8	5.491	121	-21.5	0.085	45	0.706	-39
900	0.632	-105	14.2	5.110	117	-21.0	0.089	42	0.671	-41
1000	0.629	-111	13.6	4.764	113	-20.7	0.092	39	0.641	-43
1500	0.623	-131	10.9	3.503	98	-19.7	0.103	32	0.541	-50
2000	0.618	-143	8.8	2.739	88	-19.2	0.110	29	0.492	-54
2500	0.614	-151	7.0	2.243	79	-18.8	0.115	28	0.469	-58
3000	0.611	-156	5.6	1.899	72	-18.4	0.120	27	0.461	-62
3500	0.608	-160	4.3	1.649	65	-18.1	0.125	27	0.460	-66
4000	0.604	-163	3.3	1.458	59	-17.7	0.130	27	0.465	-70

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

HEWLETT PACKARD

LINEAR POWER TRANSISTOR CHIP

HXTR-5001

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz
22 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
13.5 dB Typical at 2 GHz
8.0 dB Typical at 4 GHz

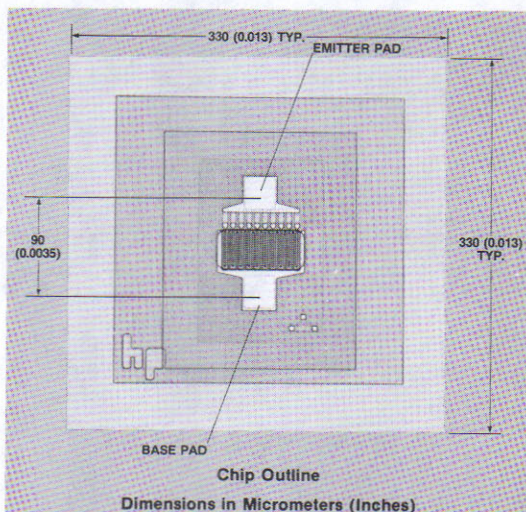
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

Description/Applications

The HXTR-5001 is an NPN bipolar transistor chip designed for high output power and gain to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5001 commend it for use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications. Programs requiring hermetically packaged devices with similar performance should employ the HXTR-5101 and the HXTR-5103 which utilize this chip.



Chip Outline
Dimensions in Micrometers (Inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Condtiions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C = 3$ mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C = 15$ mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B = 30$ μA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB} = 2$ V		3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at $V_{CE} = 32$ V		3041.1**	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB} = 20$ V		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 18$ V, $I_C = 30$ mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1 dB Gain Compression	f = 2 GHz 4 GHz		dBm		23 22	
G_{1dB}	Associated 1 dB Compressed Gain	f = 2 GHz 4 GHz		dB		13.5 8	
P_{SAT}	Saturated Power Output (8 dB Gain) (3 dB Gain)	f = 2 GHz 4 GHz		dBm		25.5 25	
η	Power-Added Efficiency at 1 dB Compression	f = 2 GHz 4 GHz		%		35 25	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP) = 22 dBm	f = 4 GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE} = 18$ V, $I_C = 30$ mA, $\Theta_{JA} = 210°C/W$						

*300 μs wide pulse measurement at ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	DC Collector Current	50 mA
P_T	Total Device Dissipation[2]	700 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175° C assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 150° C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4.0V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.4W
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

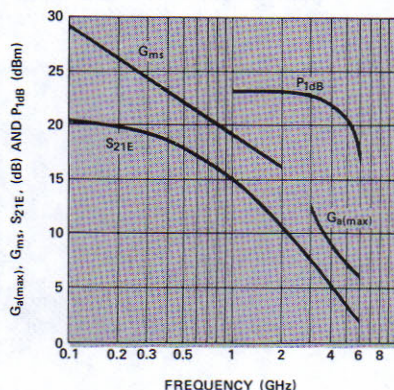


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), S_{21E}, and P_{1dB} Linear Power vs. Frequency at V_{CE} = 18V, I_C = 30 mA.

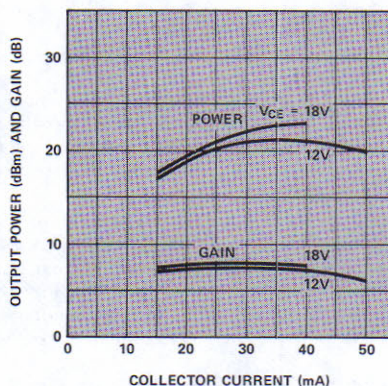


Figure 2. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Current at V_{CE} = 12V and 18V at 4 GHz.

Typical S-Parameters* V_{CE} = 18V, I_C = 30 mA

Freq. (GHz)	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
0.100	0.74	-15	20.2	10.2	171	-38	0.01	83	0.99	-5
0.200	0.73	-30	19.9	9.88	162	-33	0.02	75	0.97	-10
0.300	0.72	-44	19.5	9.42	154	-30	0.03	69	0.93	-15
0.400	0.71	-57	19.0	8.87	146	-28	0.04	63	0.89	-19
0.500	0.70	-68	18.4	8.28	140	-26	0.05	58	0.85	-22
0.600	0.69	-78	17.7	7.71	134	-25	0.06	54	0.80	-24
0.700	0.67	-87	17.1	7.16	129	-25	0.06	50	0.76	-26
0.800	0.67	-94	16.5	6.65	124	-24	0.06	47	0.73	-28
0.900	0.66	-101	15.8	6.19	120	-24	0.07	44	0.70	-29
1.000	0.65	-107	15.2	5.78	117	-23	0.07	42	0.67	-30
1.500	0.63	-128	12.6	4.25	103	-22	0.08	37	0.58	-32
2.000	0.62	-140	10.5	3.33	94	-22	0.08	35	0.53	-32
2.500	0.61	-148	8.7	2.73	87	-21	0.09	35	0.51	-33
3.000	0.61	-154	7.3	2.32	81	-21	0.09	35	0.50	-35
3.500	0.61	-158	6.1	2.02	76	-20	0.10	36	0.49	-36
4.000	0.60	-161	5.8	1.79	71	-20	0.10	37	0.49	-38
4.500	0.60	-164	4.1	1.61	66	-19	0.11	38	0.49	-40
5.000	0.60	-166	3.3	1.47	62	-19	0.11	39	0.49	-43
5.500	0.59	-168	2.6	1.35	58	-19	0.12	40	0.49	-45
6.000	0.59	-169	2.0	1.25	55	-18	0.12	40	0.49	-47

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

HEWLETT PACKARD

LINEAR POWER TRANSISTOR CHIP

HXTR-5002

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2GHz
27.5 dBm Typical at 4GHz

HIGH ASSOCIATED GAIN
12.5 dB Typical at 2GHz
7.5 dB Typical at 4GHz

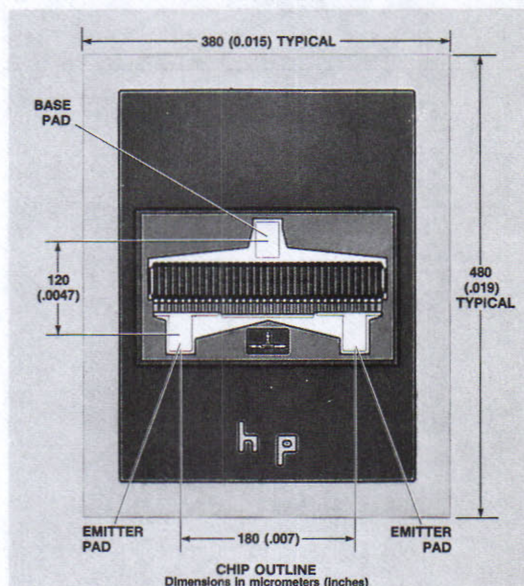
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

Description/Applications

The HXTR-5002 is an NPN bipolar transistor chip designed for high output power and gain to 5GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5002 commend it for use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications. Programs requiring hermetically packaged devices with similar performance should employ the HXTR-5102 and the HXTR-5104, which utilize this chip.



CHIP OUTLINE
Dimensions in micrometers (inches)

Gold Bonding Pad Dimensions: ~ 38 (.0015) x 20 (.0008) Typical
Chip Thickness: 90 (.0035) Typical
Collector Back Contact: Silicon-Gold Eutectic

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C=10mA$		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C=50mA$		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B=100\mu A$		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB}=2V$		3061.1	μA			5
I_{CES}	Collector-Emitter Leakage Current at $V_{CE}=32V$		3041.1**	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB}=20V$		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=18V$, $I_C=110mA$		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f = 2GHz 4GHz		dBm		29 27.5	
G_{1dB}	Associated 1dB Compressed Gain	f = 2GHz 4GHz		dB		12.5 7.5	
P_{SAT}	Saturated Power Output (8dB Gain) (3dB Gain)	f = 2GHz 4GHz		dBm		31.0 29.5	
η	Power-Added Efficiency at 1dB Compression	f = 2GHz 4GHz		%		38 23	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at $P_O(PEP)=.5W$	f = 4GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE}=18V$, $I_C=110mA$, $\Theta_{ja}=55°C/W$						

*300μsec wide pulse measurement at ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	DC Collector Current	150 mA
P_T	Total Device Dissipation[2]	2.7W
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) to below the design goal of 1×10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a θ_{JB} (Junction-to-Back contact thermal resistance) of 45°C/W.

   Total θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4W
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

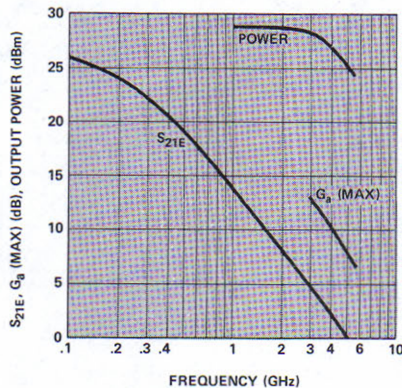


Figure 1. Typical S_{21E}, G_a(max) and P_{1dB} Linear Power vs. Frequency at V_{CE} = 18V, I_C = 110mA.

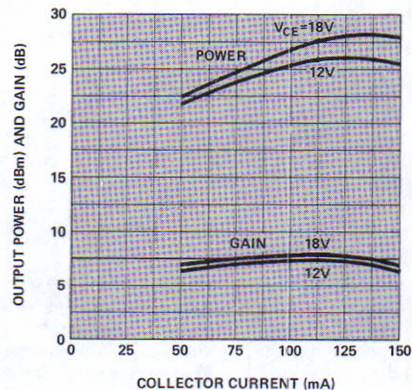


Figure 2. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

Typical S-Parameters* V_{CE} = 18V, I_C = 110mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.55	-61	25.4	19.7	156	-31.6	0.03	68	0.93	-26
0.200	0.65	-98	24.2	16.2	133	-27.3	0.04	50	0.76	-46
0.300	0.72	-119	22.3	13.1	125	-25.6	0.05	39	0.63	-60
0.400	0.76	-132	20.6	10.7	117	-24.8	0.06	32	0.53	-71
0.500	0.79	-141	19.1	9.01	111	-24.4	0.06	27	0.45	-78
0.600	0.80	-147	17.8	7.73	106	-24.1	0.06	24	0.40	-84
0.700	0.81	-151	16.6	6.74	102	-24.0	0.06	22	0.36	-89
0.800	0.81	-155	15.5	5.97	99	-23.8	0.06	20	0.33	-93
0.900	0.82	-158	14.6	5.35	97	-23.7	0.06	19	0.31	-96
1.000	0.82	-160	13.7	4.84	94	-23.7	0.06	18	0.30	-99
1.500	0.83	-167	10.3	3.29	86	-23.4	0.07	16	0.25	-109
2.000	0.83	-170	7.9	2.49	80	-23.3	0.07	16	0.24	-114
2.500	0.83	-173	6.0	2.00	74	-23.1	0.07	17	0.24	-117
3.000	0.83	-174	4.5	1.68	69	-22.9	0.07	18	0.25	-118
3.500	0.83	-175	3.2	1.44	64	-22.6	0.07	19	0.27	-119
4.000	0.83	-176	2.1	1.27	60	-22.4	0.08	20	0.28	-120
4.500	0.83	-177	1.1	1.13	55	-22.1	0.08	21	0.30	-121
5.000	0.83	-177	0.3	1.03	51	-21.9	0.08	21	0.32	-121
5.500	0.83	-178	-0.5	0.94	47	-21.6	0.08	22	0.34	-122
6.000	0.83	-178	-1.2	0.87	43	-21.4	0.08	22	0.35	-123

* (Values do not include any parasitic bonding inductances and were generated by use of a computer model.)

HEWLETT PACKARD

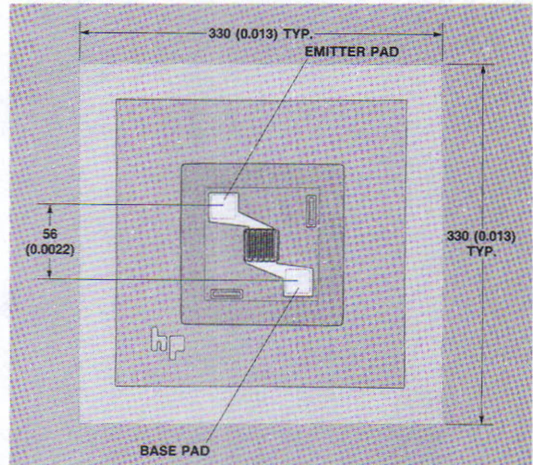
LOW NOISE TRANSISTOR CHIP

HXTR-6001

Features

LOW NOISE FIGURE
1.7 dB Typical at 2 GHz
2.7 dB Typical at 4 GHz

HIGH GAIN AT NOISE FIGURE BIAS
13.0 dB Typical at 2 GHz
9.0 dB Typical at 4 GHz



Chip Outline

Dimensions in Micrometers (Inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Description/Applications

The HXTR-6001 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave low noise performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustments. The HXTR-6001 features a Ti/Pt/Au metallization system and a dielectric scratch protection over its active area to insure reliable operation.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C=100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE}=10V$		3041.1**	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB}=10V$		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=10V$, $I_C=4mA$		3076.1*	—	50	150	250
F_{MIN}	Minimum Noise Figure	f=2 GHz	3246.1	dB		1.7	
		4 GHz				2.7	
G_a	Associated Gain	f=2 GHz				13.0	
		4 GHz				9.0	
	Conditions for above: $V_{CE}=10V$, $I_C=4mA$, $\Theta_{JA}=250°C/W$						

*300μs wide pulse measurement ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	10 mA
P_T	Total Device Dissipation[2]	150 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device median time to failure (MTTF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 150°C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	300°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

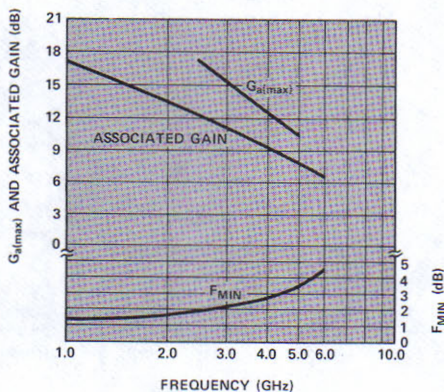


Figure 1. Typical $G_{a(max)}$, Noise Figure (F_{MIN}), and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 4mA.

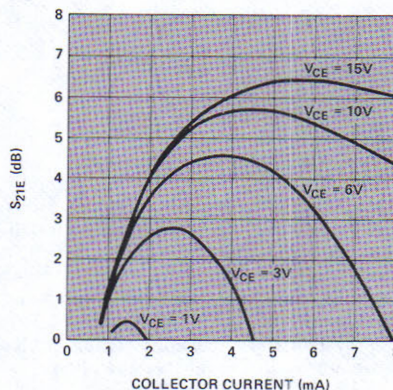


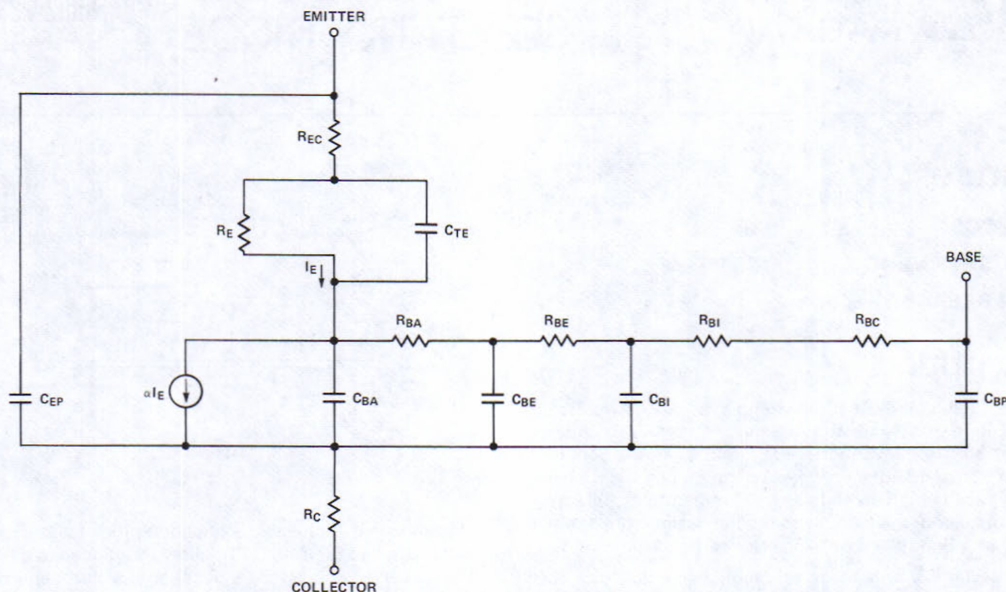
Figure 2. Typical S_{21E} vs. Current at 4 GHz.

Typical S-Parameters* V_{CE} = 10V, I_C = 4mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.87	-16	22.0	12.6	170	-46	0.005	82	0.99	-3
200	0.85	-30	21.7	12.1	160	-40	0.010	75	0.98	-5
300	0.82	-44	21.1	11.4	151	-36	0.015	68	0.95	-7
400	0.79	-57	20.5	10.6	144	-35	0.018	63	0.93	-9
500	0.76	-68	19.8	9.77	137	-34	0.021	58	0.91	-10
600	0.73	-78	19.1	9.00	131	-32	0.024	55	0.89	-10
700	0.70	-86	18.5	8.37	126	-32	0.025	52	0.87	-11
800	0.68	-94	17.6	7.62	121	-31	0.027	50	0.85	-11
900	0.66	-100	17.0	7.05	118	-31	0.028	48	0.84	-11
1000	0.65	-106	16.3	6.54	114	-31	0.029	47	0.82	-11
1500	0.60	-126	13.5	4.73	102	-29	0.034	45	0.79	-12
2000	0.58	-139	11.3	3.67	93	-29	0.037	45	0.78	-13
2500	0.57	-146	9.5	2.99	87	-28	0.041	47	0.77	-14
3000	0.56	-152	8.1	2.53	82	-27	0.045	49	0.77	-15
3500	0.56	-156	6.8	2.19	77	-26	0.049	51	0.76	-16
4000	0.55	-159	5.7	1.93	72	-26	0.053	52	0.76	-18
4500	0.55	-162	4.8	1.73	68	-25	0.057	53	0.76	-19
5000	0.55	-164	3.9	1.57	65	-24	0.062	54	0.76	-21
5500	0.55	-165	3.2	1.44	61	-24	0.066	55	0.76	-23
6000	0.54	-167	2.5	1.34	57	-23	0.071	55	0.76	-24
7000	0.54	-169	1.4	1.17	51	-22	0.080	56	0.77	-28

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

BIPOLAR CHIP EQUIVALENT CIRCUIT [1]



CURRENT DEPENDENT CURRENT SOURCE

$$\alpha = \frac{\alpha_o}{1 + j\, f/f_b} \exp(-j\, 2\, \pi\, f\, \tau)$$

$$\alpha_o = \frac{H_{fe}}{1 + H_{fe}}$$

$$R_e\, \alpha = \frac{\alpha_o}{1 + (f/f_b)^2} \left[\cos(2\pi f \tau) - \frac{f}{f_b} \sin(2\pi f \tau)\right]$$

$$Im\, \alpha = \frac{-\alpha_o}{1 + (f/f_b)^2} \left[\sin(2\pi f \tau) + \frac{f}{f_b} \sin(2\pi f \tau)\right]$$

NOTE: 1. This equivalent circuit is for the transistor chip only. It does not include parasitic bonding reactances. For additional information, please refer to "Low-Noise Microwave Bipolar Transistor with Sub-Half-Micrometer Emitter Width" by Tzu-Hwa Hsu and Craig P. Snapp, IEEE Transactions on Electron Devices, Vol. ED-25, No. 6, June 1978.

BIPOLAR CHIP EQUIVALENT CIRCUIT ELEMENTS

DEVICE	C_{BP} (pF)	C_{EP} (pF)	C_{BI} (pF)	C_{BE} (pF)	C_{BA} (pF)	C_{TE} (pF)	R_{EC} (Ω)	R_{BI} & R_{BC} (Ω)	R_{BE} (Ω)	R_{BA} (Ω)	R_C (Ω)	R_E (Ω)	α_o	f_b GHz	τ psec.
HXTR-6001 10V, 4 mA	0.053	0.05	0.019	0.016	0.0055	1.03	0.7	0.4	7.8	6.1	7	8.6	0.990	22.7	12.1
HXTR-2001 15V, 25 mA	0.066	0.06	0.07	0.056	0.032	4.8	0.2	0.2	3.5	4.4	5	1.0	0.990	22.7	10.8
HXTR-2001 15V, 15 mA	0.066	0.06	0.07	0.056	0.032	4.8	0.2	0.2	3.5	4.4	5	1.7	0.990	22.7	10.6
HXTR-5001 18V, 30 mA	0.065	0.06	0.07	0.053	1.034	5.1	7.2	.2	5.6	4.7	5	0.86	0.976	22.7	10.8
HXTR-5002 18V, 110 mA	0.105	0.15	0.22	0.18	0.11	17.3	3.1	0.2	1.7	1.4	3	0.24	0.976	22.7	10.9

Hybrid Integrated Circuits

HEWLETT PACKARD

BEAM LEAD SCHOTTKY DIODE

5082-2837

Features

LOW COST

FAST SWITCHING

HIGH BREAKDOWN

Description

The HP 5082-2837 is an epitaxial planar passivated Beam Lead Diode whose construction utilizes a unique combination of both a conventional PN junction and a Schottky barrier. This manufacturing process results in a device which has the high breakdown and temperature characteristics of silicon, the turn-on voltage of germanium and the speed of a Schottky diode majority carrier device.

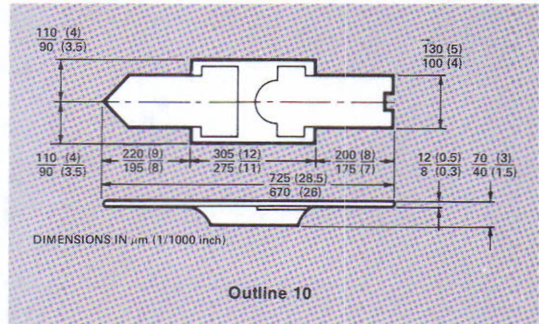
This device is intended for high volume, low cost applications, and is the beam lead equivalent of the HP 5082-2800 glass packaged diode.

Applications

High level detection, switching, or gating; logarithmic or A-D converting; sampling or wave shaping are jobs the 5082-2837 will do better than conventional PN junction diodes. The low turn-on voltage and subnanosecond switching makes it extremely attractive in digital circuits for DTL gates, pulse shaping circuits or other low level applications. Its high PIV allows wide dynamic range for fast high voltage sampling gates.

The 5082-2837 low turn-on voltage gives low offsets. The extremely low stored charge minimizes output offsets caused by the charge flow in the storage capacitor. At UHF, the diodes exhibit 95% rectification efficiencies. Both their low loss and their high PIV allow the diodes to be used in mixer and modulator applications which require wide dynamic ranges.

The combination of these technical features with the low price make these devices the prime consideration for any hybrid dc or RF circuit requiring nonlinear elements.



Outline 10

Absolute Maximum Ratings at T_A=25°C

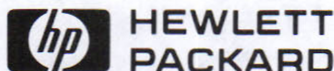
Operating Temperature Range ...... -60°C to +150°C
Storage Temperature Range .... -60°C to +150°C
Maximum Lead Pull .... 2 Gms

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

Electrical Specifications at T_A=25°C

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	70	–	Volts	I_R = 10µA
Forward Voltage	V_{F1}	–	410	mV	I_{F1} = 1mA
Forward Voltage	V_{F2}	–	1.0	V	I_{F2} = 15mA
Reverse Leakage Current	I_R	–	200	nA	V_R = 50V
Capacitance	C_o	–	2.0	pF	V_R = 0V and f= 1MHz
Effective Minority Carrier Lifetime	τ	–	100 *	pS	I_F = 5mA Krakauer Method

* Typical.



BEAM LEAD SCHOTTKY DIODES FOR MIXERS AND DETECTORS (1-18 GHz)

HSCH-5300 SERIES

Features

PLATINUM TRI-METAL SYSTEM
Higher Temperature, Stronger Leads

NITRIDE PASSIVATION
Stable, Reliable Performance

LOW NOISE FIGURE
6 dB Typical at 9 GHz

HIGH UNIFORMITY
Tightly Controlled Process Insures Uniform RF Characteristics

RUGGED CONSTRUCTION
4 Grams Minimum Lead Pull

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

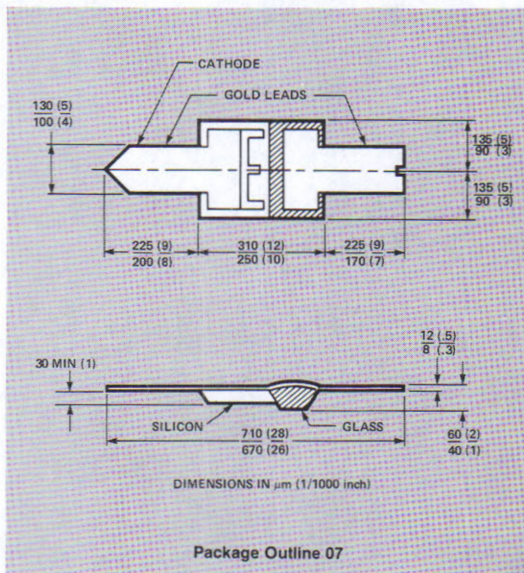
The HP beam lead process allows for large beam anchor pads for rugged construction (typical 6 gram pull strength) without degrading capacitance.

Maximum Ratings

Pulse Power Incident at $T_A = 25°C$ 1W
CW Power Dissipation at $T_A = 25°C$ 300mW
T_{OPR} — Operating Temperature
Range .... -60° C to +175° C
T_{STG} — Storage Temperature
Range .... -60° C to +200° C
Minimum Lead Strength .... 4 grams pull on either lead
Diode Mounting Temperature ... 300° C for 10 sec. max.

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.



Package Outline 07

Applications

The beam lead diode is ideally suited for use in stripline or microstrip circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through Ku-band.

The basic medium barrier devices in this family are DC tested HSCH-5310, -5312, and -5316. Batch matched versions are available as the HSCH-5311, -5313, and -5317. Equivalent low barrier devices are HSCH-5330, -5332 and -5336. Batch matched versions are available as HSCH-5331, -5333, and -5337.

For applications requiring guaranteed RF performance, the HSCH-5318 is selected for 6.2 dB maximum noise figure at 9.375 GHz, with RF batch match units available as the HSCH-5319. The HSCH-5314 is rated at 7.2 dB maximum noise figure at 16 GHz with RF batch match units available as the HSCH-5315.

For low-barrier RF performance, the HSCH-5338 and -5334 are selected for noise figure 6.2 dB maximum at 9.375 and 7.2 dB maximum at 16 GHz respectively. Batch matched versions are available as the HSCH-5339 and -5335.

Electrical Specifications for RF tested Diodes at $T_A = 25°C$

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Maximum Total Capacitance C_T (pF)	Typical Forward Voltage V_F (mV)
5318	5319	Medium	6.2 at 9.375 GHz	200	400	1.5:1	4	12	0.25	450
5314	5315		7.2 at 16 GHz					18	0.15	
5338	5339	Low	6.2 at 9.375 GHz	200	400	1.5:1	4	12	0.25	300
5334	5335		7.2 at 16 GHz					18	0.15	
Test Conditions	ΔNF≤0.3dB $ΔZ_{IF}$≤25Ω		DC Load Resistance = 0Ω L.O. Power = 1 mW I_F = 30 MHz, 1.5 dB NF				I_R = 10 μA	I_F = 5 mA	V_R = 0V f = 1 MHz	I_F = 1 mA

*Minimum batch size 20 units.

Electrical Specifications for DC tested Diodes at $T_A = 25°C$

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Maximum Total Capacitance C_T (pF)	Typical Forward Voltage V_F (mV)
5316	5317	Medium	4	12	0.25	450
5312	5313			18	0.15	
5310	5311			25	0.10	
5336	5337	Low	4	12	0.25	300
5332	5333			18	0.15	
5330	5331			25	0.10	
Test Conditions	$ΔV_F$ ≤ 15 mV @ 5 mA		I_R = 10 μA	I_F = 5 mA	V_R = 0V f = 1 MHz	I_F = 1 mA

*Minimum batch size 20 units.

Typical Detector Characteristics at $T_A = 25°C$

MEDIUM BARRIER

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20μA Bias
Detection Sensitivity	γ	6.6	mV/μW	Video Bandwidth = 2 MHz
Video Resistance	Rv	1400	Ω	f = 10 GHz

LOW BARRIER (ZERO BIAS)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-44	dBm	Zero Bias
Detection Sensitivity	γ	10	mV/μW	Video Bandwidth = 2 MHz
Video Resistance	Rv	1.8	MΩ	f = 10 GHz

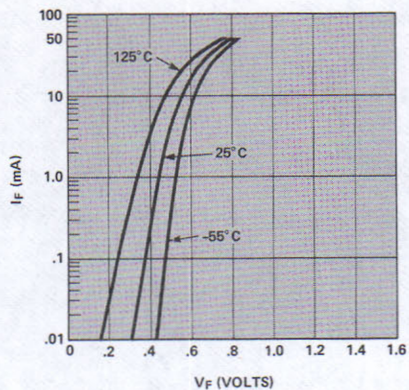


Figure 1. Typical Forward Characteristics, for Medium Barrier Beam Lead Diodes. HSCH-5310 Series.

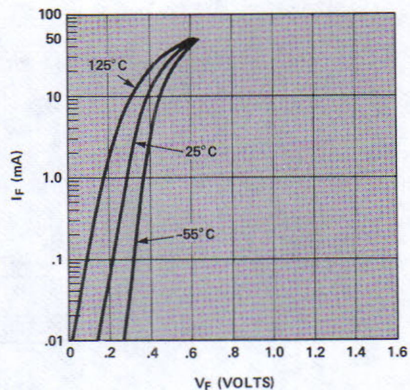


Figure 2. Typical Forward Characteristics, for Low Barrier Beam Lead Diodes. HSCH-5330 Series.

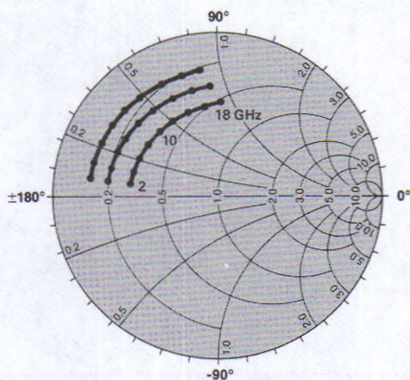


Figure 3. Typical Admittance Characteristics, with Self Bias. HSCH-5314, -5315, -5334, and -5335.

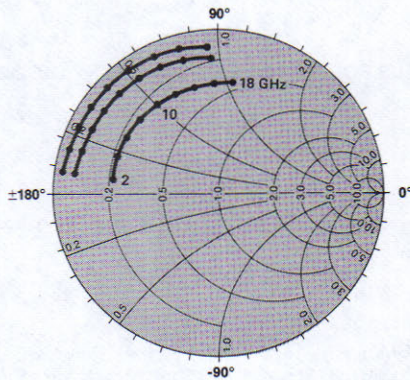


Figure 4. Typical Admittance Characteristics, with External Bias. HSCH-5314, -5315, -5334, and -5335.

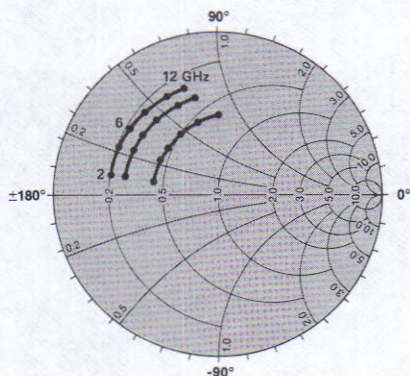


Figure 5. Typical Admittance Characteristics, with Self Bias. HSCH-5318, -5319, -5338 and -5339.

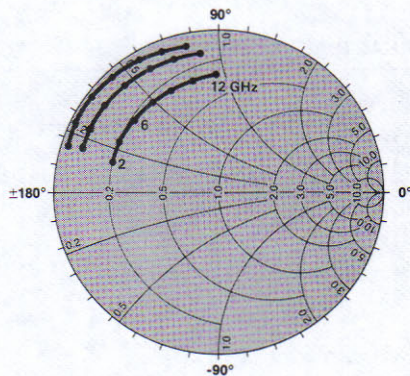


Figure 6. Typical Admittance Characteristics, with External Bias. HSCH-5318, -5319, -5338 and -5339.

Hybrid Integrated Circuits

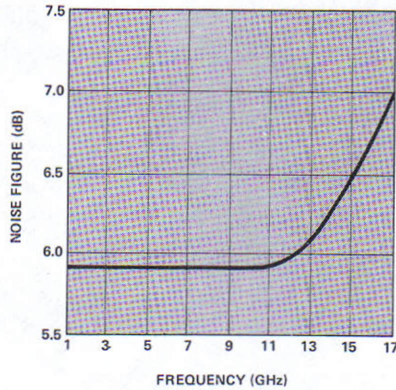
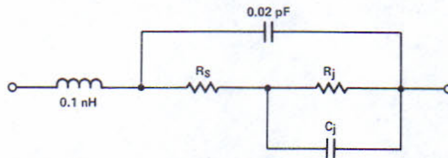


Figure 7. Typical Noise Figure vs. Frequency.

NOTES:
1. 1 μs pulse, Du = .001.
2. Power absorbed by the diode. DC load resistance < 1Ω.

MODELS FOR BEAM LEAD SCHOTTKY DIODES



SELF BIAS

Part Numbers	1.0 mA Self Bias			1.5 mA Self Bias			3.0 mA Self Bias		
	R_S	R_j	C_j	R_S	R_j	C_j	R_S	R_j	C_j
HSCH-5314, -5315, -5334, -5335	5.0	393	0.11	5.2	232	0.11	5.0	150	0.12
HSCH-5318, -5319, -5338, -5339	5.1	244	0.16	5.0	178	0.16	5.0	109	0.19

EXTERNAL BIAS

Part Numbers	20 μADC Bias			50 μADC Bias			150 μADC Bias		
	R_S	R_j	C_j	R_S	R_j	C_j	R_S	R_j	C_j
HSCH-5314, -5315, -5334, -5335	2.8	1240	0.11	4.7	618	0.12	2.7	211	0.13
HSCH-5318, -5319, -5338, -5339	5.1	2050	0.18	3.9	665	0.19	4.7	242	0.20

HEWLETT PACKARD

BEAM LEAD SCHOTTKY DIODE QUADS FOR DOUBLE BALANCED MIXERS (1-18 GHz)

5082-9394-9399
5082-9696-9697

Features

PLANAR SURFACE
Easier Bonding, Stronger Leads

NITRIDE PASSIVATED
Stable, Reliable Performance

HIGH UNIFORMITY
Tightly Controlled Process Insures Uniform RF Characteristics

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor.

During manufacturing, gold leads are deposited onto a glass passivation layer before the wafer is separated. This provides exceptional lead strength.

These monolithic arrays of Schottky diodes are interconnected in ring configuration. The relative proximity of the diode junctions on the wafer assures uniform electrical characteristics among the four diodes which constitute a matched quad. They are designed for microstrip or stripline use. The leads provide a good continuity of transmission line impedance to the diode.

Applications

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size.

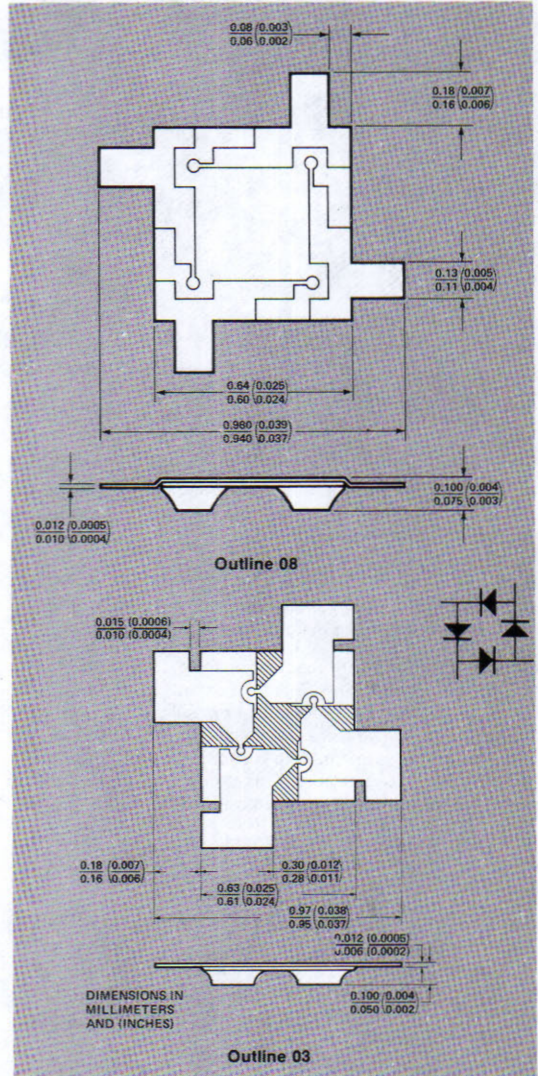
Maximum Ratings

Junction Operating and Storage Temperature Range .... -65° C to +150° C

DC Power Dissipation at 25° C .... 75 mW/Junction
Derate linearly to zero at $T_{j(op)}$ max.
(Measured in infinite heat sink)

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.



Hybrid Integrated Circuits

Selection Guide

Package Outline \ Frequency	Barrier	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
Beam Lead	Medium	5082-9696	5082-9696	5082-9394	5082-9396	5082-9398
	Low	5082-9697	5082-9697	5082-9395	5082-9397	5082-9399

Electrical Characteristics at $T_A = 25°C$ / Typical Parameters

Part Number 5082-	Outline	Maximum Capacitance C_T (pF)	Maximum Capacitance Difference ΔC_T (pF)	Maximum Dynamic Resistance R_D (Ω)	Forward Voltage V_F(V)[2]
9697	08	0.55	0.10	12	0.25
9395	08	0.35	0.10	15	0.25
9397	03	0.20	0.05	16	0.30
9399	03	0.15	0.05	16	0.30
9696	08	0.55	0.10	12	0.35
9394	08	0.35	0.10	15	0.35
9396	03	0.20	0.05	16	0.45
9398	03	0.15	0.05	16	0.45
Test Conditions		$V_R = 0$ f = 1 MHz[1]		I_F = 5 mA Measured Between Adjacent Leads.	I_F = 1 mA Measured Between Adjacent Leads.

Notes:
1. Measured between diagonal leads.
2. Maximum ΔV_F = 20mV at I_F = 5 mA measured between adjacent leads.

Handling Instructions

The mechanical and electrical performance characteristics of beam lead diodes require careful and considerate handling during inspection, testing, and assembly. The handling techniques described here are necessary so that the diodes will not be mechanically or electrically damaged. The diodes are very small and magnification may be necessary to see them inside the shipping container.

Hewlett-Packard beam lead diodes are shipped in a flat, plastic container. The inside bottom surface of the container is coated with a thin layer of silicone to which the diodes adhere. They are covered with anti-static silk. A vacuum pickup with a #27 tip is recommended for picking up single beam lead devices. This should be done under 20x magnification for accurate positioning of the tip on the die.

A beam lead diode can be destroyed electrically by a static discharge through the diode. Hence, they must be handled so static discharges cannot occur.

If a vacuum pickup is not used, it is recommended that a wooden toothpick or sharpened Q-tip dipped in alcohol be used as a handling probe. A diode will adhere to the end of the wooden probe without danger of mechanically or electrically damaging the diode. It can then be placed where needed.

If tweezers are used, they must be electrically grounded to the surface upon which the device is being placed. The tweezer part should be dulled and used as a probe to lift the diodes and should not be used to grasp the diode. If used as tweezers to hold the diode, the gold tabs can be deformed.

Bonding Recommendations

Beam lead devices are silicon chips with coplanar plated gold tabs that extend parallel to the top surface of the chip approximately 8 mils beyond the edge. The leads are approximately 4 mils wide by 1/2 mil thick and are mounted by thermocompression bonding to the substrate metallization. The bonding is accomplished by placing the device face down with the tabs resting flat on the pad area and using heated wedge (and/or substrate)* or parallel-gap (spot-welding) techniques.

The heated wedge may be continuously heated, as in most standard equipment, or it may be pulse resistance heated where a high current, short duration pulse is used to raise the wedge to the required temperature. In the spot-welding operation, current is passed through the substrate metallization and the device lead. Most of the heat is generated at the interface between the two, where the bond is formed.

The major advantage of pulse heating techniques is that a cold ambient may be used, generating only localized heating in the vicinity of the bond itself. The electrodes (or wedge) can be placed on the device lead while the bond area is cold, and maintain a constant force through the heating and cooling cycle.

*Typical conditions for thermocompression bonding are:
Stage Temperature: 130° C-190° C
Wedge Temperature: 300° C
Pressure: 125 Grams
Time: 3 seconds maximum

For further details see AN 974, Die Attach and Bonding Techniques for Diodes & Transistors.

Schottky Barrier Diodes

SCHOTTKY BARRIER DIODES FOR GENERAL PURPOSE APPLICATIONS

ELECTRICAL SPECIFICATIONS AT T_A = 25° C

Part Number 5082-			Nearest Equivalent Packaged Part No. 5082-	Nearest Equivalent Beam Lead Part No. 5082-	Minimum Breakdown Voltage, V_{BR} (V)	Minimum Forward Current I_F (mA)	Maximum Junction Capacitance C_{jo} (pF)
Chip For Epoxy Or Solder Die Attach	Chip For Eutectic Die Attach	Lid (Outline 50)					
0024	0094	2802	2800	2837	70	15	1.7
0087	0057		2810		20	35	1.0
0097	0058		2811		15	20	1.1
0031			2835		8*	10*	0.8
300° C 1 Min.	400° C 1 Min.	250° C 5 Sec.	Soldering Conditions				
Notes: [1,2,3]	[1,2]	[4] C_P = .18 pF			I_R = 10 µA *I_R = 100 µA	V_F = 1V *V_F = 0.45V	V_R = 0V f = 1 MHz

Note: Total Capacitance $C_{TO} = C_{jo} + C_P$.

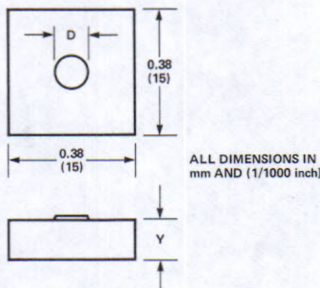
SCHOTTKY BARRIER DIODES FOR MIXING AND DETECTING

ELECTRICAL SPECIFICATIONS AT T_A = 25° C — TYPICAL PARAMETERS

Part Number 5082-		Nearest Equivalent Packaged Part No. 5082-	Nearest Equivalent Beam Lead Part No. 5082-	Maximum Junction Capacitance Cjo (pF)	Typical Noise Figure NF (dB)[B]	Typical Tangential Sensitivity TSS (dBm)
Chip	LID (Outline 50)					
0023		2713	2709	0.18	6.0	-54
0029		2721	2716		6.0 7.0*	-54
0013[A,C]		HSCH-3206[C] -2285[A]	2299[A,C]	0.13		-42[C] -54[A]
HSCH-5017[C]		HSCH-5019[C]		0.35		-54
0009	2754	2750		0.1	7.0	-55
250° C, 1 Min. or 300° C, 15 Sec.	250° C 5 Sec.	Soldering Conditions				
Notes [1, 5]	[45] C_P = .18 pF			V_R = 0V f = 1 MHz	f = 9.375 GHz *f = 16 GHz	I_{BIAS} = 20 µA f = 10 GHz BW = 2 MHz

Notes: A. Low V_F Schottky Barrier Diodes. B. NF includes 1.5 dB for the IF Amplifier. C. Zero bias.

Outline Drawing



For LID drawing see page 198.
The 5082 prefix does not apply to part numbers containing HSCH.

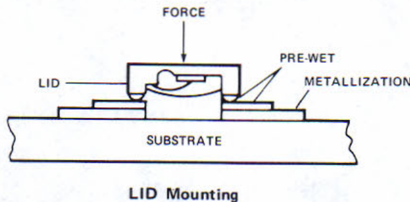
Dimension	HP Part Number 5082-				
	0024 0094	0057, 0058, 0087, 0097	0031	0013, 0023,* 0029	HSCH-5017 0009*
D	0.10 (4)	0.08 (3)	0.06 (2.5)	0.02 (0.80)	
Y	0.13 (5)			0.10 (4)	
Top Contact	Au, Anode	Au, Anode	Au, Anode	Au, Anode	Au, Cathode
Bottom Contact	Au, Cathode	Au, Cathode	Au, Cathode	Au, Cathode	Au, Anode
Oper. & Stg. Temp. Range	-65° C to +200° C		-65° C to +150° C		

DIMENSIONS IN MILLIMETERS (1/1000 inch)
*9 contact versions are available as 5082-0041 (5082-0023) and 5082-9891 (5082-0009).

Hybrid Integrated Circuits

Notes:

1. Use standard thermocompression bonding techniques. Ultrasonic bonding is not recommended.
2. Thermal compression bonding is recommended for attaching wires or mesh to Schottky barrier diode chips. The carrier should be placed on a stage heated to 220° C-240° C. Heat and pressure may be applied to the wire by the edge of a capillary such as Tempress 5102-20 heated to 280° C-300° C. A force of 25-30 grams should be applied for 5 seconds.
3. Eutectic bonding or die attaching may damage the chip. A preform must be used.
4. Leadless Inverted Device (LID). Mounting recommendations: the LID may be mounted by individually soldering each device or batch flow soldered as illustrated below:

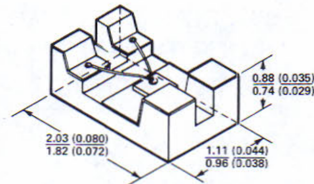


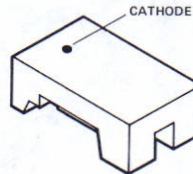
LID Mounting

Prior to soldering it is advisable to tin each device. Scrub the pads of the LID with a Pink Pearl eraser to remove any dirt or other foreign matter. Then rinse the LID in TCE (Trichloroethylene).

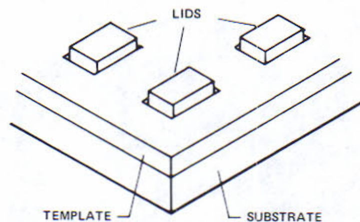
Dip the LID in Alpha 711 Flux using titanium tweezers. With those tweezers, place the unit in a solder bath of 62% Sn, 36% Pb, and 2% Ag, for 30 seconds and remove. Note, the solder bath must be maintained at a temperature of 220° C plus or minus 5° C through the process.

Dip the LID in the solder bath again for 3 seconds. When removing the LID, hold it 1/8 inch above the solder pot for 5 seconds to obtain thermal equilibrium. Wait 10 seconds before rinsing in TCE. Brush off the TCE with an artist's brush.





Outline 50 (LID Package)



Batch Reflow Soldering of LIDs

Now inspect each LID under a microscope to see if the tin covers over 90% of the contact pad area and if this area appears to have a shiny, bright, continuous homogeneous solder casting. If the LID appearance fails to meet the inspection criteria, repeat the tinning process, starting with the flux dip.

5. Handle with grounded tweezers and grounded bonding equipment. These diodes are pulse sensitive and may be damaged by electrostatic charges.

HEWLETT PACKARD

BEAM LEAD PIN DIODE

5082-3900

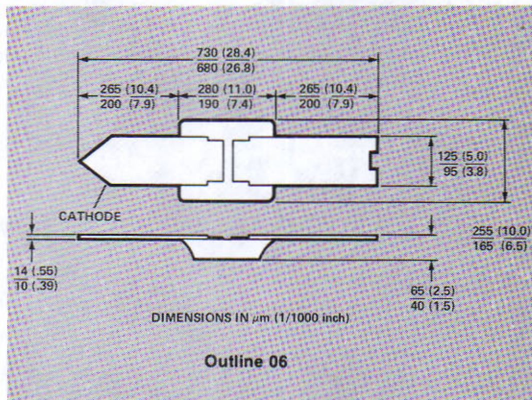
Features

HIGH BREAKDOWN VOLTAGE
200 V

LOW CAPACITANCE
0.02 pF

RUGGED CONSTRUCTION
2 Grams Minimum Lead Pull

NITRIDE PASSIVATED



Outline 06

Description/Applications

The HP 5082-3900 Beam Lead PIN diodes are constructed to offer exceptional lead strength while achieving excellent electrical performance at microwave frequencies.

The HP 5082-3900 Beam Lead PIN diode is designed for use in stripline or microstrip circuits using welding or thermocompression bonding techniques. PIN applications include switching, attenuating, phase shifting, limiting and modulating at microwave frequencies.

Maximum Ratings at T_{CASE}=25°C

Junction Operating Temperature .... -65°C to +150°C
Storage Temperature .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

Diode Mounting Temperature ... 220°C for 10 sec. max.
Power Dissipation .... 250 mW
(Derate linearly to zero at 150°C)
Minimum Lead Strength ... 2 Grams Pull on Either Lead

Hybrid Integrated Circuits

Electrical Specifications at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Breakdown Voltage	V_{BR}	150	200	–	V	I_r = 10μA
Series Resistance	Rs	–	6	8	ohm	I_f=50mA, f=100MHz
Capacitance	C_O	–	.02	.025	pF	V = 0V, f = 3GHz
Minority Carrier Lifetime	τ	–	150	–	ns	I_f=50mA, I_r=250mA

Typical Parameters

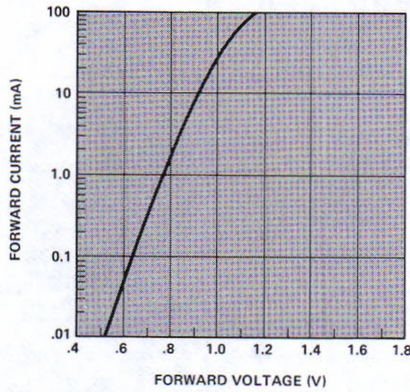


Figure 1. Typical Forward Conduction Characteristics.

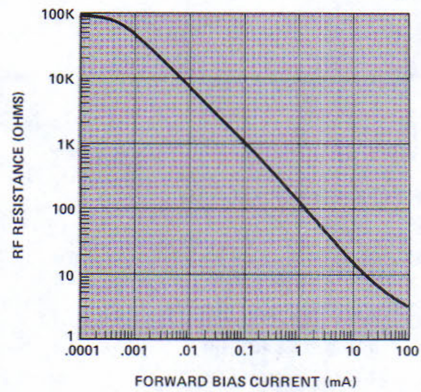


Figure 2. Typical RF Resistance vs. DC Bias Current.

HEWLETT PACKARD

LOW LOSS BEAM LEAD PIN DIODES

HPND-4001 HPND-4050

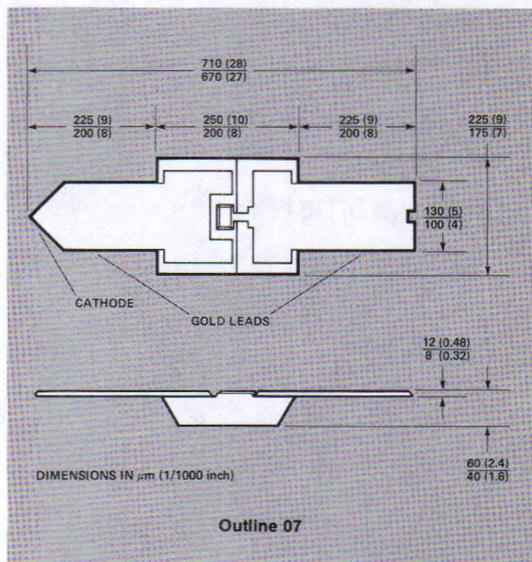
Features

LOW SERIES RESISTANCE
1.3Ω Typical

LOW CAPACITANCE
0.07 pF Typical

FAST SWITCHING
2 ns Typical

RUGGED CONSTRUCTION
4 Grams Minimum Lead Pull



Outline 07

Description /Applications

The HPND-4001 and -4050 are beam lead PIN diodes designed specifically for low capacitance, low series resistance and rugged construction. The new HP mesa process allows the fabrication of beam lead PINs with a very low RC product. A nitride passivation layer provides immunity from contaminants which would otherwise lead to I_R drift. A deposited glass layer (glassivated) provides scratch protection.

The HPND-4001 and -4050 beam lead PIN diodes are designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting and modulating at microwave frequencies. The low capacitance and low series resistance at low current make these devices ideal for applications in the shunt configuration.

Bonding Techniques

Thermocompression bonding is recommended. The stage should be heated to 220°C and the bonding tool to 300°C maximum. Bonding time should not exceed 10 seconds. Either welding or ultrasonic bonding could also be used. For additional information, see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy."

Hybrid Integrated Circuits

Electrical Specifications at T_A=25°C

Part Number	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)		Capacitance C_T (pF)		Minority Carrier Lifetime τ (ns)	Reverse Recovery Time t_{rr} (ns)
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Typ.	Typ.
HPND-4001	50	80	1.8	2.2	0.07*	0.08*	30	3
HPND-4050	30	40	1.3	1.7	0.12	0.15	15	2
Test Conditions	$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$		I_F = 10 mA f = 100 MHz		V_R = 10 V *V_R = 30V f = 1 MHz		I_F = 10 mA I_R = 6 mA	I_F = 10 mA V_R = 10V

Maximum Ratings at $T_{CASE} = 25°C$

Operating Temperature .... -65° C to +175° C
Storage Temperature .... -65° C to +200° C

Operation of these devices within the above temperature ratings will assure a device Median Time To Failure (MTTF) of approximately 1 x 10^7 hours.

Power Dissipation .... 250 mW
(Derate linearly to zero at 175° C)
Minimum Lead Strength .... 4 grams pull on either lead

Typical Parameters

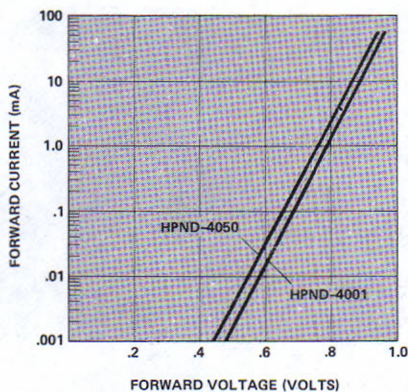


Figure 1. Typical Forward Characteristics.

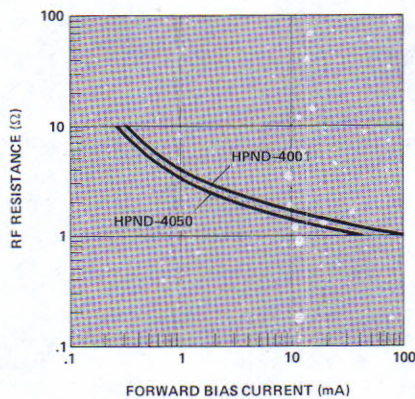


Figure 2. Typical RF Resistance vs. Forward Bias Current.

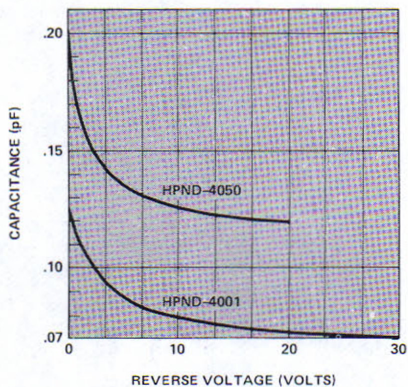


Figure 3. Typical Capacitance vs. Reverse Voltage.

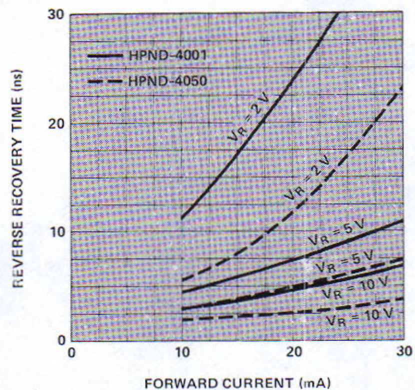


Figure 4. Typical Reverse Recovery Time vs. Forward Current (Shunt Configuration)

HEWLETT PACKARD

BEAM LEAD PIN DIODE

HPND-4005

Features

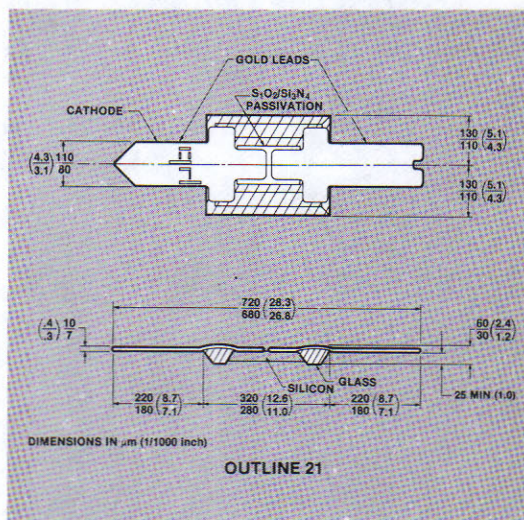
HIGH BREAKDOWN VOLTAGE
120V Typical

LOW CAPACITANCE
0.017 pF Typical

LOW RESISTANCE
4.7Ω Typical

RUGGED CONSTRUCTION
4 Grams Minimum Lead Pull

NITRIDE PASSIVATED



OUTLINE 21

Description/Applications

The HPND-4005 planar beam lead PIN diodes are constructed to offer exceptional lead strength while achieving excellent electrical performance at microwave frequencies.

The HPND-4005 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, limiting and modulating at microwave frequencies. The extremely low capacitance of the HPND-4005 makes it ideal for circuits requiring high isolation in a series diode configuration.

Bonding Techniques

Thermocompression bonding is recommended but welding, ultrasonic bonding or conductive epoxy can also be used. For additional information, see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy."

Hybrid Integrated Circuits

Electrical Specifications at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Breakdown Voltage	V_{BR}	100	120	—	V	$I_R = 10\ \mu A$
Series Resistance	R_S	—	4.7	6.5	Ohm	$I_F = 20$ mA, f = 100 MHz
Capacitance	C_{VR}	—	.017	.02	pF	$V_R = 10V$, f = 10 GHz
Minority Carrier Lifetime	τ	—	150	—	ns	$I_F = 50$ mA, $I_R = 250$ mA
Reverse Recovery Time	t_{rr}	—	20	—	ns	$I_F = 20$ mA, $V_R = 10$ V, 90% Recovery

*Total capacitance calculated from measured isolation value in a series configuration.

Maximum Continuous Ratings at T_{CASE} = 25°C

Operating Temperature .... −65°C to +175°C

Storage Temperature .... −65°C to +200°C

Operation of these devices within the above temperature ratings will assure a device median time to failure (MTTF) of approximately 1 x 10^7 hours.

Power Dissipation .... 250 mW
(Derate linearly to zero at 175°C)

Minimum Lead Strength .... 4 grams pull on either lead

Diode Mounting Temperature .... 220°C for 10 seconds maximum

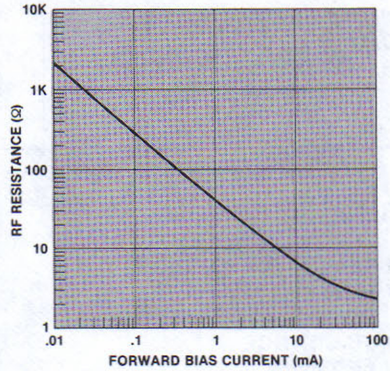


Figure 2. Typical RF Resistance vs. Forward Bias Current.

Typical Parameters

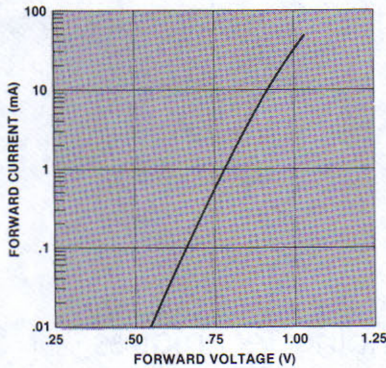


Figure 1. Typical Forward Conduction Characteristics.

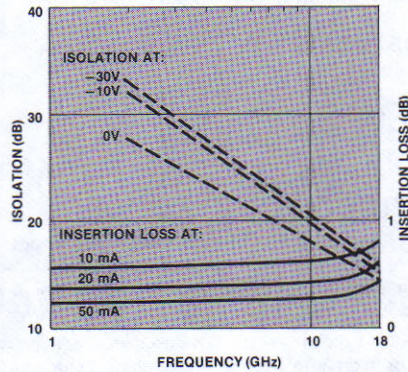


Figure 3. Typical Isolation and Insertion Loss in the Series Configuration (Z_O = 50Ω)

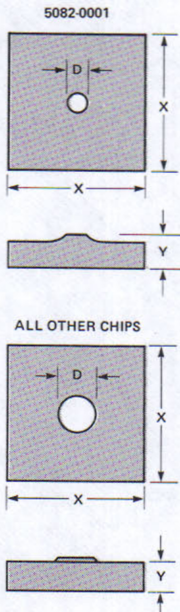
PIN Diodes

ELECTRICAL SPECIFICATIONS AT $T_A = 25°C$ | **TYPICAL PARAMETERS**

Part Number 5082- Chip	LID (Outline 50)	Ministrip (Outline 72)	Post (Outline 74)	Nearest Equivalent Packaged Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Junction Capacitance C_{JVR} (pF)	Typical Series Resistance R_S (Ω)	Typical Lifetime τ (ns)	Typical Reverse Recovery Time, t_{rr} (ns)
0012	3005	3000	3259	3001	150	0.12	0.8	400	100
0030				3301	150	0.12	0.8	400	100
0047				3001	150	0.15	0.6	400	100
0001*			3258	3041	70	0.16	0.8*	15	5
0025				3080	100	0.20	1.5	1300	1000
0039				3081	100	0.20	2.0	2000	1000
0049				3046	400	0.20	0.6	1000	200
0034				3168	35	1.2	0.4**	40	12
425°C 1 Min. *300°C 1 Min.	250°C 5 Sec.	325°C 5 Sec.	250°C 5 Sec.	Soldering Conditions					
[1*, 2]	[3, 4] C_P = .18 pF	[5] C_P = .13 pF	[6] C_P = .13 pF		$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	V_R = 50V *V_R = 20V f = 1 MHz	I_F = 100 mA *I_F = 20 mA **I_F = 10 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	I_F = 20 mA V_R = 10V

Note: Total capacitance $C_{TO} = C_{JVR} + C_P$.

Outline Drawings



Dimension	HP Part Number 5082- 0012 0047	0030	0034	0025	0039	0049	0001
D	0.10 (4)			0.23 (9)	0.24 (9.5)		0.06 (2.5)
X	0.38 (15)			0.51 (20)			0.38 (15)
Y	0.09 (3.5)		0.13 (5)	0.15 (6)	0.23 (9)	0.08 (3.2)	0.11 (4.5)
Top Contact	Au, Cathode	Au, Anode	Au, Anode	Ag, Cathode			Au, Anode
Bottom Contact	Au, Anode	Au, Cathode		Au, Anode			Au, Cathode

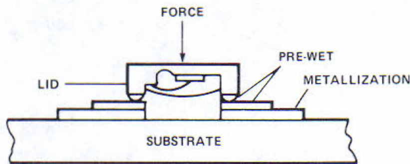
DIMENSIONS IN MILLIMETERS (1/1000 inch)

Operating and Storage Temperature Range -60°C to +150°C

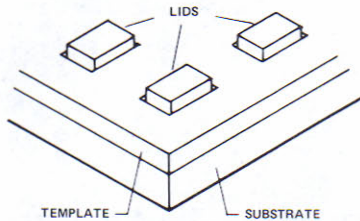
For LID and Ministrip drawings see page 206.

Notes:

1. Use standard thermocompression bonding techniques. Ultrasonic bonding is not recommended.
2. Either ultrasonic or thermocompression bonding techniques can be employed.
3. Polarity Designation on LID's. See outline 50 (LID Package.
4. Leadless Inverted Device (LID). Mounting recommendations: the LID may be mounted by individually soldering each device or batch flow soldered as illustrated below:



LID Mounting



Batch Reflow Soldering of LIDs

Prior to soldering it is advisable to tin each device. Scrub the pads of the LID with a Pink Pearl eraser to remove any dirt or other foreign matter. Then rinse the LID in TCE (Trichloroethylene).

Dip the LID in Alpha 711 Flux using titanium tweezers. With those tweezers, place the unit in a solder bath of 62% Sn, 36% Pb, and 2% Ag, for 30 seconds and remove. Note, the solder bath must be maintained at a temperature of 220° C plus or minus 5° C through the process.

Dip the LID in the solder bath again for 3 seconds. When removing the LID, hold it 1/8 inch above the solder pot for 5 seconds to obtain thermal equilibrium. Wait 10 seconds before rinsing in TCE. Brush off the TCE with an artist's brush.

Now inspect each LID under a microscope to see if the tin covers over 90% of the contact pad area and if this area appears to have a shiny, bright, continuous homogeneous solder casting. If the LID appearance fails to meet the inspection criteria, repeat the tinning process, starting with the flux dip.

5. Ministrip Handling and Mounting Techniques. The ministrips may be mounted by using conductive epoxy such as Hysol K20 or Dupont 5504. Conventional soldering techniques may also be used.

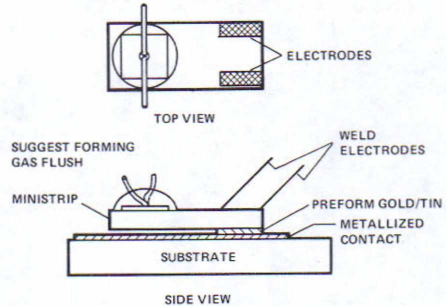
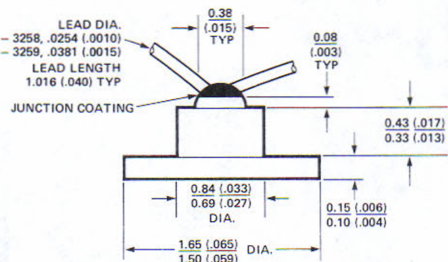


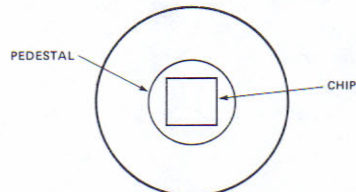
Figure 1. Resistance Heating the Ministrip

Direct heating or resistive heating of the substrate using a parallel gap welder are acceptable methods. High temperature solder preforms such as gold-tin (280° C Eutectic) may be used.

The composition of the solder preform should be compatible with the techniques and materials used in the substrate and conductive land patterns.

The leads may be attached by using ultrasonic or thermocompression bonding methods. A parallel gap welder may also be used. Conventional soldering techniques are not recommended for the gold leads.





CHIP CENTER IS WITHIN 0.08 (.003) OF PEDESTAL CENTER

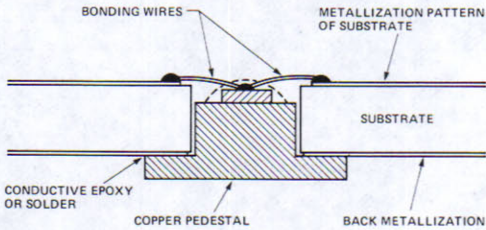
ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 74 (Post)

The HP package outline 74 consists of a gold plated copper pedestal. The top contact wire exhibits an inductance (L_P) of approximately .5 nH for a typical connecting wire length of approximately 20 mils.

The polarity of the 5082-3258 is cathode on heat sink. The polarity of the 5082-3259 is anode on heat sink.

After attachment of a gold wire, the chip is covered with a thin layer of silicon junction coating for protection against mechanical damage. The connecting wires are bent upwards for transportation and easy circuit insertion.



Suggested Microstrip Assembly Technique

Hybrid Integrated Circuits

Step Recovery Diodes

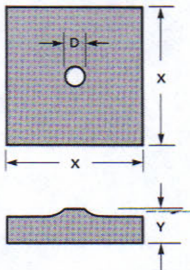
ELECTRICAL SPECIFICATIONS AT T_A = 25° C

Part Number 5082-		
Chip	**Ministrip (Outline 72)**	**Minimum Breakdown Voltage, V_{BR}(V)**
0020	0305	25
0008	0340	15
0032	0307	65
0090	—	45
0021	0308	40
0015	0306	35
0017	0364	75
0018	0309	25
300° C 1 Min.	250° C 5 Sec.	—
[1]	[2] Cp = .13 pF	I_R = 10 μA

TYPICAL PARAMETERS

Chip Capacitance C_{jVR}(pF)	Lifetime τ(ns)	Transition Time t_r(ps)	Charge Level (pc)	Nearest Equivalent Packaged Part No. 5082-
0.4-1.0	20	60	300	0830
0.15-0.5	10	50	100	0835
4.0	150	250	1500	0241
1.0	50	80	300	0820
2.0	100	150	1000	0310
1.2	60	150	1000	0132
4.0	300	300	2400	0300
0.5	20	70	200	0253
—	—	—	—	Soldering Conditions
V_R = 10V f = 1 MHz	—	—	—	Notes

Outline Drawings



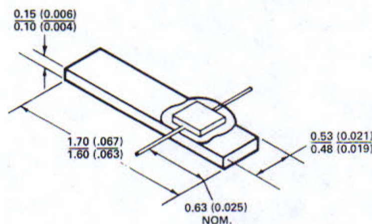
DIMENSIONS IN MILLIMETERS (1/1000 inch)

Dimension	5082- 0200	0008	0015	0017	0018	0021	0032	0090
D	0.10 (4)	0.06 (2.5)	0.15 (6)	0.39 (15.5)	0.05 (2)	0.22 (8.5)	0.32 (12.5)	0.15 (6)
X	0.38 (15)	0.38 (15)	0.38 (15)	0.64 (25)	0.38 (15)	0.51 (20)	0.51 (20)	0.38 (15)
Y	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)

Top Contact: Ag, Anode

Bottom Contact: Au, Cathode

Operating and Storage Temperature Range
-60° C to +200° C



*71 MINISTRIP HAS ONLY ONE LEAD.

Outline 71,72

ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

Notes:

1. Either ultrasonic or thermocompression bonding techniques can be employed.
2. Ministrip Handling and Mounting Techniques. The Ministrips may be mounted by using conductive epoxy such as Hysol K20 or Dupont 5504. Conventional soldering techniques may also be used.

   Direct heating or resistive heating of the substrate using a parallel gap welder are acceptable methods. High temperature solder preforms such as gold-tin (280° Eutectic) may be used for the Step Recovery and PIN diodes. Low temperature solder preforms such as tin-lead should be used with the Schottky barrier diodes. The composition of the solder preform should be compatible with the techniques and materials used in the substrate and conductive land patterns.

   The leads may be attached by using ultrasonic or thermocompression bonding methods. A parallel gap welder may also be used (Figure 1). Conventional soldering techniques are not recommended for the gold leads.

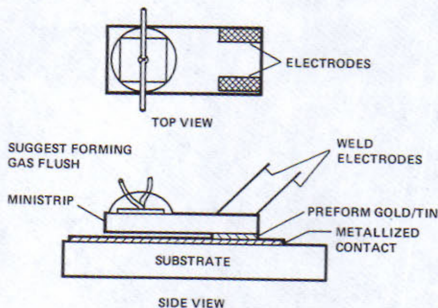


Figure 1. Resistance Heating the Ministrip

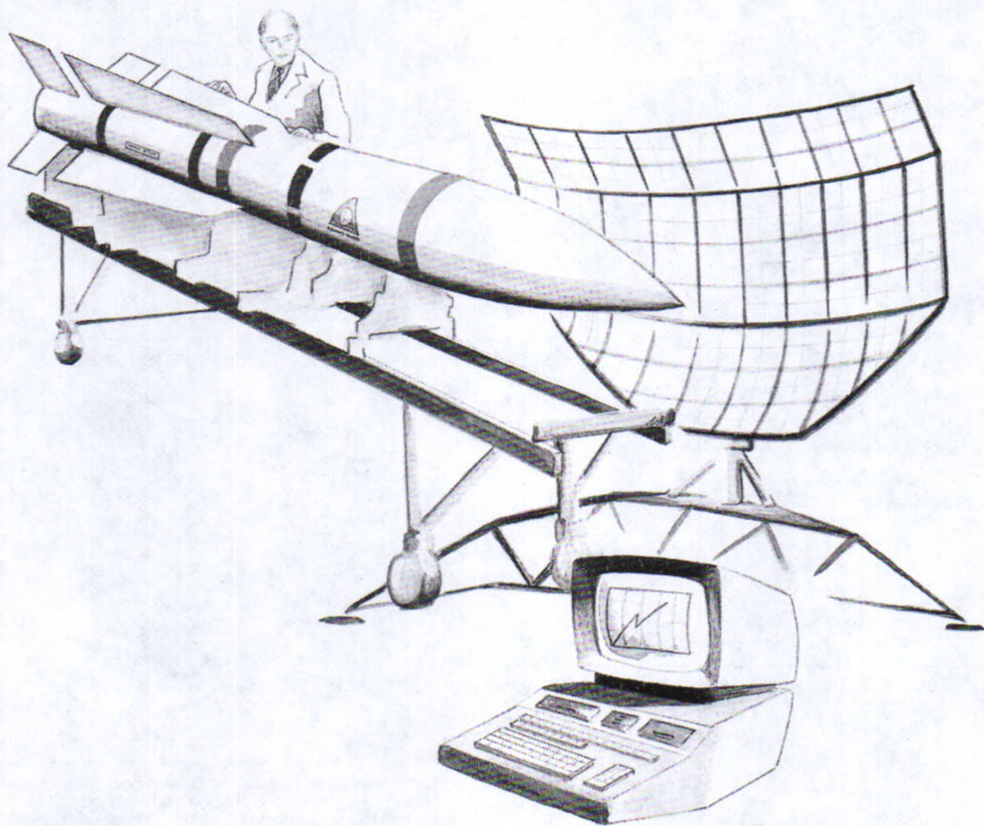
Hybrid Integrated Circuits

Applications for Devices for Hybrid Integrated Circuits

The Beam Lead Mesa PIN in Shunt Applications 212

The Handling and Bonding of Beam Lead Devices Made Easy 213

Achieve High Isolation in Series with the Low Capacitance HPND-4005 Beam Lead PIN 214



The Beam Lead Mesa PIN in Shunt Applications (Portion of AN 971)

INTRODUCTION

The low RC product, fast switching time, and other unique features of the HPND-4050 beam lead PIN diode make it well suited for switching applications in the shunt configuration. Proper choice and optimum design of circuit to minimize parasitics and loss will allow these inherent characteristics of the HPND-4050 to be exploited to the fullest and achieve maximum performance.

SWITCHING PERFORMANCE

The actual performance of the HPND-4050 as a shunt switch is illustrated in Figures 1 and 2. The points denoted by Δ are results of a computer analysis yielding the equivalent circuit shown in Figure 3. It can be observed that isolation actually increases with frequency up to X-band due to shunt capacitance before it rolls off as lead inductance dominates. Insertion loss increases steadily with frequency as a result of shunt capacitance. This data confirms the importance of low parasitics and a low RC product.

The fast switching time observed is shown in Figure 4. To switch from an isolation state with forward bias of 10 mA to a transmission (insertion loss) state with reverse bias of −10 volts, less than 1 nanosecond is required. Much less than 1 nanosecond is needed to switch from a transmission to an isolation state.

OTHER TOPICS

Practical circuits, handling, and bonding suggestions are also discussed in this application note.

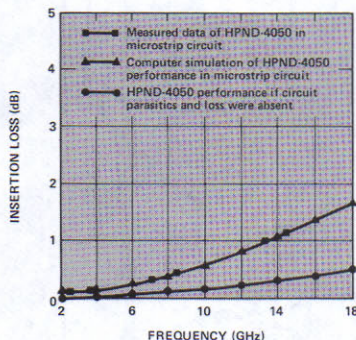


Figure 1. Insertion Loss of HPND-4050 as Shunt Switch.

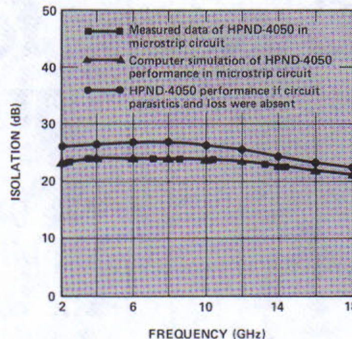
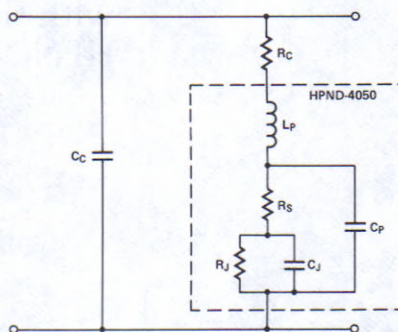


Figure 2. Isolation of HPND-4050 as Shunt Switch.



SYMBOL	PARAMETER	SWITCH "ON"	SWITCH "OFF"	UNITS
R_c	Circuit Resistance	.5	.5	Ω
C_c	Circuit Capacitance	.12	.12	pF
L_p	Package Inductance	.02	.02	nH
C_p	Package Capacitance	.02	.02	pF
R_s	Series Resistance	.5	.5	Ω
R_j	Junction Resistance	20K	.8	Ω
C_j	Junction Capacitance	.1	20	pF

Figure 3. Equivalent Circuit of HPND-4050 in Microstrip Circuit.

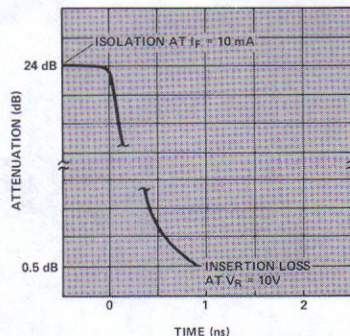


Figure 4. Beam Lead Mesa PIN Switching Time. For the beam lead mesa PIN in shunt to switch from an isolation state with forward bias of 10 mA to an insertion loss state with reverse bias of −10V less than 1 ns is required.

The Handling and Bonding of Beam Lead Devices Made Easy

(Portion of AN 979)

INTRODUCTION

Beam lead devices are particularly suited for hybrid integrated circuits where low parasitics and small size are prime requirements. Available as single units or monolithic quads, the beam lead devices have made high packing density and superior performance easily achievable in hybrid circuits.

HANDLING

In order to avoid damage to the mechanical and electrical characteristics of beam lead devices, particular care must be exercised in the handling of these devices during inspection, testing, and assembly. Although the construction of the beam lead devices is designed to have exceptional lead strength, the small size and delicate nature of the devices require that special handling techniques be observed so that the devices would not be mechanically or electrically damaged.

A vacuum pickup (Figure 1) is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle be sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

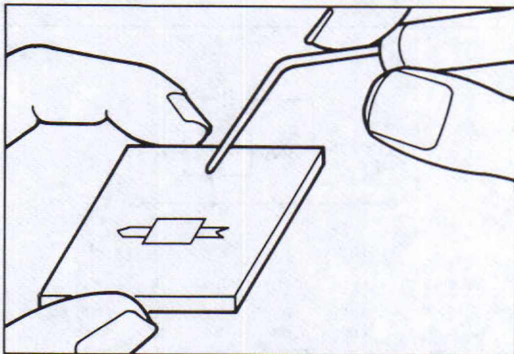


Figure 1. Vacuum Pickup is Suitable, for Beam Lead Devices, Particularly Larger Ones, e.g., Quads.

BONDING

Thermocompression bonding is recommended for the beam lead devices. Parallel-gap welding can also be used. In either method, the device is positioned face down as illustrated in Figure 2 with the beam leads resting flat on the metalized contact areas of the circuit and bonded using either a heated wedge (thermocompression bonding) or parallel-gap (welding) technique.

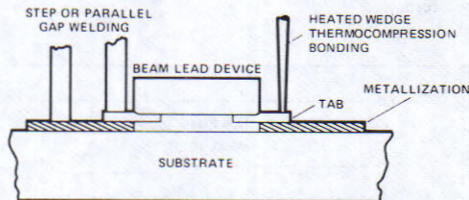


Figure 2. The Bonding of the Beam Lead Device is Achieved Using Either a Heated Wedge (Thermocompression Bonding) or Parallel Gap (Welding) Technique.

Many commercially available bonders are specifically designed or can be adpated to bond beam lead devices. Shown in Figure 3 is an example of one such bonder which is the Unitek Model 8-150-02 bonder.

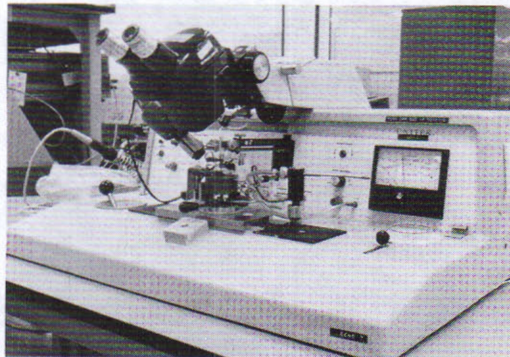


Figure 3. The Unitek Model 8-150-02 Bonder is Adaptable for the Thermocompression Bonding of Beam Lead Devices.

Other suggestions for the handling and bonding of beam lead devices are found in this application note.

Achieve High Isolation in Series Applications with the Low Capacitance HPND-4005 Beam Lead PIN (Portion of AN 985)

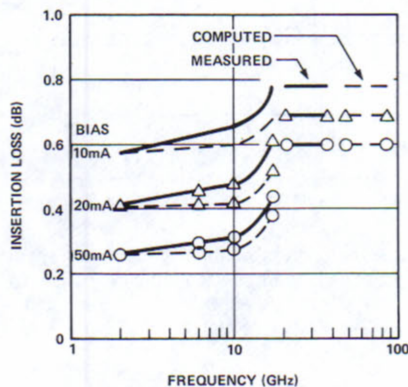
INTRODUCTION

The HPND-4005 beam lead PIN is designed primarily for use in stripline or microstrip circuits. Applications include switching, attenuating, modulating, phase shifting, and other signal control functions at microwave frequencies in test instrumentation, communication, electronic warfare, navigational, and phased array radar systems. The extremely low capacitance and low resistance of this diode make it particularly suited for circuits requiring high isolation and low insertion loss in the series diode configuration. In this application note the capabilities of this diode as a series switching element will be demonstrated in a SPST (single pole single throw) and a SPDT (single pole double throw) circuit.

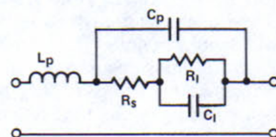
SERIES SWITCHING PERFORMANCE

The actual performance of the HPND-4005 as a series switch was measured in a circuit which consisted of a 50 Ohm coplanar transmission line built on a 25 mil alumina substrate ($\epsilon_r = 10$). Figure 1 (A) shows the insertion loss based on both the measured performance of the actual circuit and the computed performance of the equivalent circuit shown in Figure 1 (B). In Figure 2 (A) are the isolation characteristics of both the actual (measured) circuit and the equivalent (computed) circuit shown in Figure 2 (B).

Other details of this SPST switch and the SPDT switch are included in this application note.



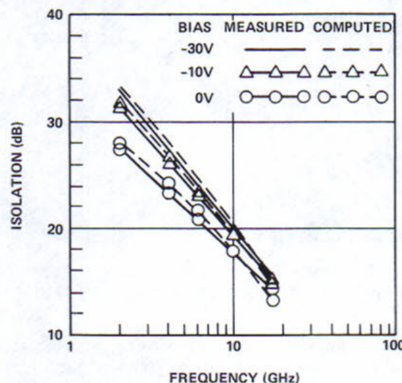
(A) INSERTION LOSS



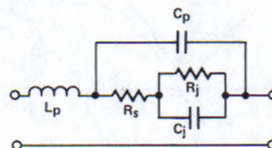
BIAS (mA)	L_p (nH)	C_p (pF)	R_s (Ω)	R_I (Ω)	C_I (pF)
10	0.15	0.009	2	4.8	0.011
20	0.15	0.009	2	2.7	0.011
50	0.15	0.009	2	0.8	0.011

(B) EQUIVALENT CIRCUIT

Figure 1. Forward Biased Characteristics of the HPND-4005 as a Series Switch.



(A) ISOLATION



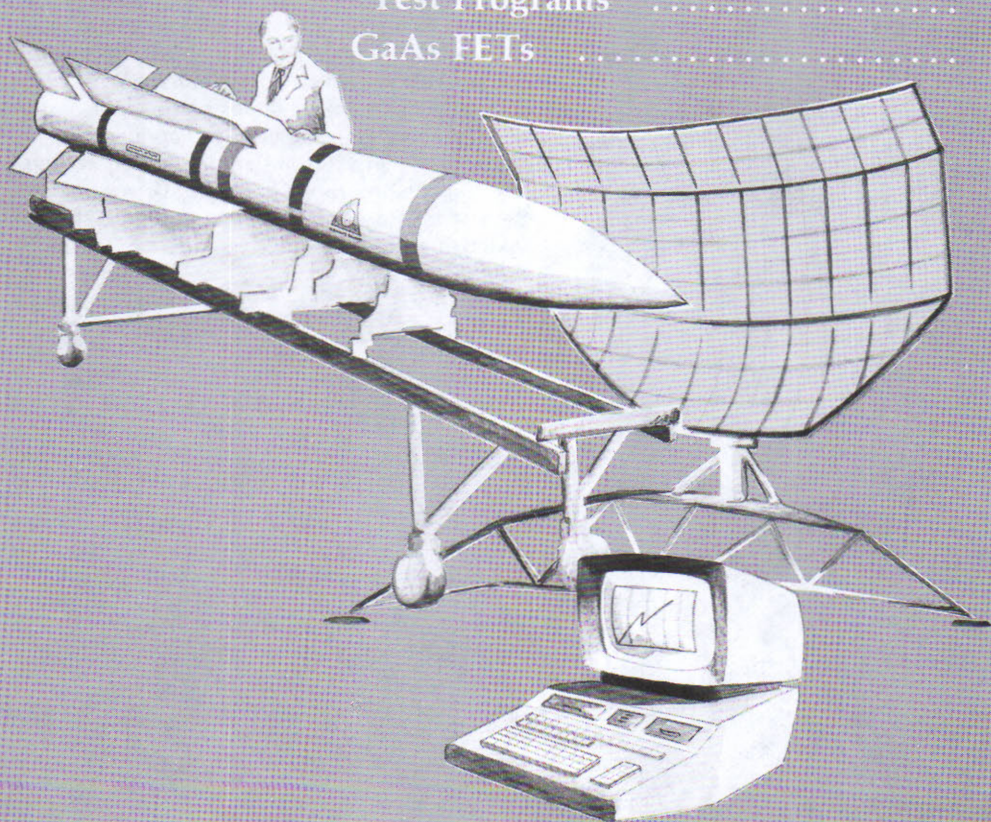
BIAS (V)	L_p (nH)	C_p (pF)	R_s (Ω)	R_j (KΩ)	C_j (pF)
-30	0.15	0.009	2	10	0.0065
-10	0.15	0.009	2	7	0.008
0	0.15	0.009	2	3	0.011

(B) EQUIVALENT CIRCUIT

Figure 2. Reverse Biased Characteristics of the HPND-4005 as a Series Switch.

High Reliability Tested Products

Introduction 216
Selection Guide 217
Schottky Switching Diode Military Approved MIL-S-19500/444 218
Schottky Switching Diode Military Approved MIL-S-19500/445 220
PIN Switching Diode Military Approved MIL-S-19500/443 222
Standard High Reliability Test Programs 224
GaAs FETs 228



High Reliability Test Philosophy

Each product accepted for commercial sale has been tested for reliability throughout the development phase and is subject to quality assurance procedures during the manufacturing process. High reliability products are subjected to additional screening to remove devices subject to early failure modes.

Military Products

Since a great number of reliability tested devices are used in military programs, the JAN (Joint Army-Navy) system has been established by the U.S. government to provide standardized levels of reliability at minimum cost to all users. There are two major advantages to the JAN type of system. First, the specification, and thus the reliability level of the device, is pre-specified for the buyer, eliminating costly creation of special procurement documents. Second, JAN devices can be manufactured in large quantities with subsequent cost reductions.

There are three levels of JAN devices:

1. JAN—
   Shipment lots have had Group B tests performed successfully on a sample basis.
2. JAN TX —
   The shipment lots have been subjected to 100% screening tests. Individual devices have been serialized, and drift data has been recorded. Group B sample data is then done after screening.
3. JAN TXV —
   These are the same level as JAN TX with the additional requirement of a pre-closure visual inspection.

Since the advantages of products tested to well established reliability standards can be of significant value to reliability oriented customers, HP makes available a number of products that have been tested to the same reliability level as the JAN type devices, but have HP part numbers and meet HP designated electrical specifications. These are our "TX" products. Typical screening programs are set forth in the TX data sheets.

Space Performance

For over 15 years, MSD has been extensively involved in many military and space oriented High Reliability Test programs. The inherent reliability and proven performance of our products has provided a vehicle with which to build a strong record of performance in the demanding requirements of space programs. By having a large group of Marketing and Product Assurance personnel dedicated to the service of High Reliability customers, HP has been frequently called upon to provide the high performance, highly reliable components demanded by many military and commercial space probe and satellite programs. Among the many space programs using HP Microwave Semiconductor Division products are Apollo, Viking, and Intelsat.

High Reliability
PIN and Schottky Diodes Selection Guide

Commercial Part Number 5082-	Military Approved JAN/JANTX/JANTXV*	Page Number
2800	1N5711	218
2810	1N5712	220
3039**	1N5719**	222

* JANTXV approval does not apply to the 1N5719.

**See page 132 for minor specification differences.

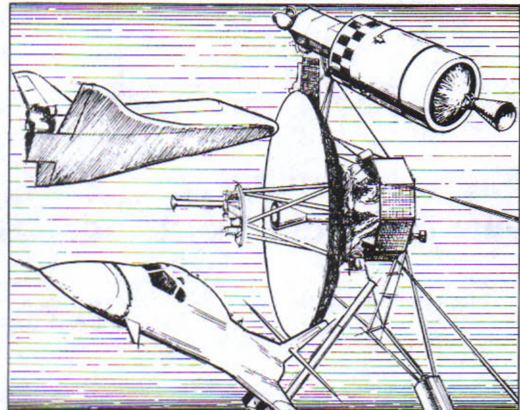
HEWLETT PACKARD

SCHOTTKY SWITCHING DIODE MILITARY APPROVED MIL-S-19500/444

JAN 1N5711
JANTX 1N5711
JANTXV 1N5711

Features

HIGH BREAKDOWN VOLTAGE
PICO-SECOND SWITCHING SPEED
LOW TURN-ON



Description/Applications

The JAN Series 1N5711 is an epitaxial, planar passivated Schottky Barrier Diode designed to have pico-second switching speed. These devices are well suited for high level detecting, mixing, switching, gating and converting, video detecting, frequency discriminating, sampling, and wave shaping applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at T_{CASE}=25°C

Operating and Storage Temperature Range .... -65°C to 200°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1 x 10^7 hours.

Reverse Voltage (Working) .... 50 V (peak)
Power Dissipation .... 250 mW
Derate at 1.43 mW/°C for T_{CASE} = 25°C to 200°C; assumes an infinite heat sink.

Electrical Specifications at T_A=25°C (Unless Otherwise Specified)

(Per Table I, Group A Testing of MIL-S-19500/444)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	70	—	V	I_R = 10μA
Forward Voltage	V_{F1}	—	.41	V	I_{F1} = 1 mA
Forward Voltage	V_{F2}	—	1.0	V	I_{F2} = 15mA
Reverse Leakage Current	I_R	—	200	nA	V_R = 50V
Reverse Leakage Current	I_R	—	200	μA	V_R = 50V, T_A = +150°C
Capacitance	$C_{T(o)}$	—	2.0	pF	V_R = 0V and f = 1 MHz
Effective Minority Carrier Lifetime	τ	—	100	pS	I_F = 5 mA Krakauer Method [Note 1]

Note 1: Per DESC drawing C-68001

JAN 1N5711: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/444.

JANTX 1N5711: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/444***. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5711 above.

JANTXV 1N5711: Devices are subject to 100% visual inspection in accordance with MIL-S-19500/444 prior to being subjected to TX screening.

Group B Sample Acceptance Tests**	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051C
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Gross Leak Test	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Temperature Storage (200°C, 1K hrs.)	1031
Operating Life I_o = 33mAdc, V_r = 50V [pk] (f = 60Hz, T_A = 25°C, t = 1K hrs.)	1026

Group C Sample Acceptance Tests**	Method MIL-STD-750
Low Temp. Operation (−65°C)	
Forward Voltage	4011
Breakdown Voltage	4021
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051C
TX Screening (100%)	
High Temp. Storage (200°C, 48 hrs.)	1032
Thermal Shock	1051C
Constant Acceleration	2006
Fine Leak	1071G or H
Gross Leak	1071E
Burn-In I_o = 33mAdc, V = 50V [pk] (T_A = 25°C, f = 60Hz, t = 96hrs)	
Evaluation of Drift (I_R, V_F)	

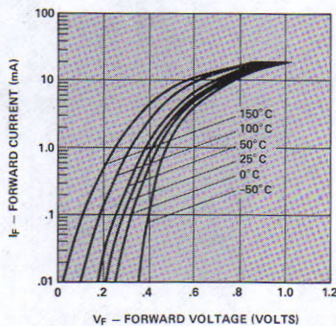
*MIL-STD-202, Method 215

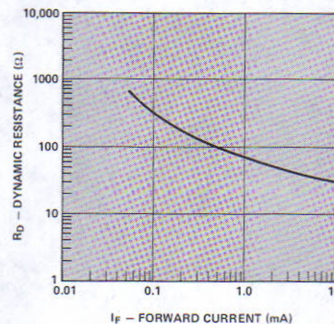
**Endpoint measurements and examinations per MIL-S-19500/444.

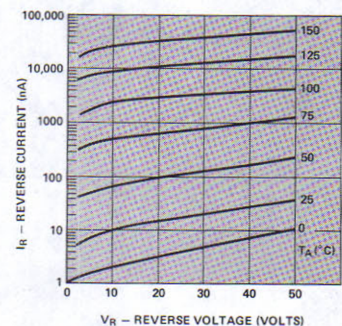
***JANTX and JANTXV devices have gold plated leads.

High Reliability Products

Typical Parameters







HEWLETT PACKARD

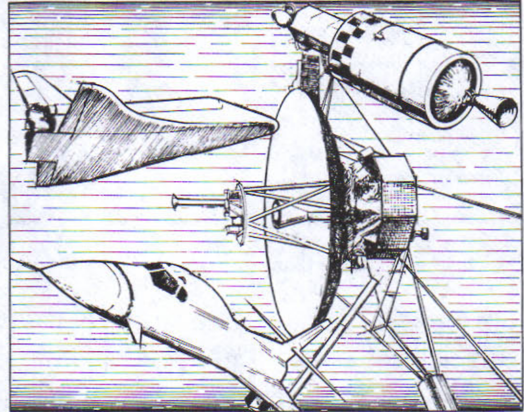
SCHOTTKY SWITCHING DIODE MILITARY APPROVED MIL-S-19500/445

JAN 1N5712
JANTX 1N5712
JANTXV 1N5712

Features

PICO-SECOND SWITCHING SPEED

LOW TURN-ON VOLTAGE



Description/Applications

The JAN Series 1N5712 is an epitaxial, planar passivated Schottky Barrier Diode designed to have pico-second switching speed. These devices are well suited for high level detecting, mixing, switching, gating, A-D converting, video detecting, frequency discriminating sampling and wave shaping applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at $T_{CASE}=25°C$

Operating and Storage Temperature
Range .... -65°C to 200°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1 x 10^7 hours.

Reverse Voltage (Working) .... 16V (peak)
Power Dissipation .... 250 mW
Derate at 1.43 mW/°C for T_{CASE} = 25°C to 200°C; assumes an infinite heat sink.

Electrical Specifications at $T_A=25°C$

(Per Table I, Group A Testing of MIL-S-19500/445)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	20		V	I_R = 10μA
Forward Voltage	V_{F1}		.55	V	I_{F1} = 1 mA
Forward Voltage	V_{F2}		1.0	V	I_{F2} = 35 mA
Reverse Leakage Current	I_R		150	nA	V_R = 16V
Capacitance	$C_{T(o)}$		1.2	pF	V_R = 0V and f = 1 MHz
Effective Minority Carrier Lifetime	τ		100	pS	I_F = 5 mA Krakauer Method [Note 1]

Note 1: Per DESC drawing C-68001

JAN 1N5712: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/445.

JANTX 1N5712: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/445. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5712 above.

JANTXV 1N5712: Devices are subject to 100% visual inspection in accordance with MIL-S-19500/445 prior to being subjected to TX screening.

Group B Sample Acceptance Tests **	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051C
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Gross Leak Test	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Temperature Storage (200°C, 1K hrs.)	1031
Operating Life I_o = 33mAdc, V_r = 16V [pk] (f = 60Hz, T_A = 25°C, t = 1K hrs.)	1026

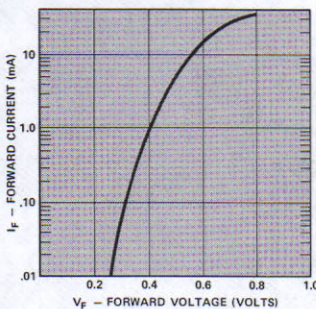
Group C Sample Acceptance Tests **	Method MIL-STD-750
Low Temp. Operation (−65°C)	
Forward Voltage	4011
Reverse Breakdown Voltage	4021
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051C
TX Screening (100%)	
High Temp. Storage (200°C, 48 hrs.)	1032
Thermal Shock	1051C
Constant Acceleration	2006
Fine Leak	1071G or H
Gross Leak	1071E
Burn-In I_o = 33mAdc, V = 16V [pk] (T_A=25°C, f=60Hz, t=96hrs.)	
Evaluation of Drift (I_R, V_F)	

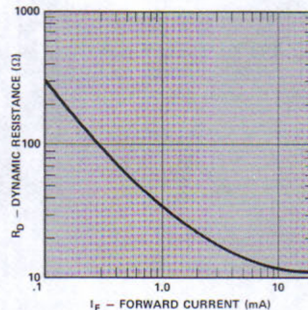
*MIL-STD-202, Method 215

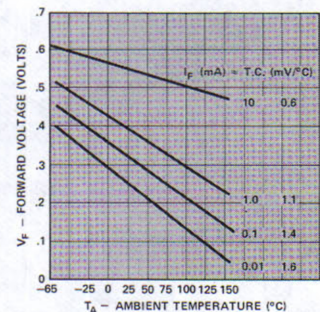
**Subgroup endpoint measurements and examinations per MIL-S-19500/445.

High Reliability Products

Typical Parameters







HEWLETT PACKARD

PIN SWITCHING DIODE MILITARY APPROVED MIL-S-19500/443

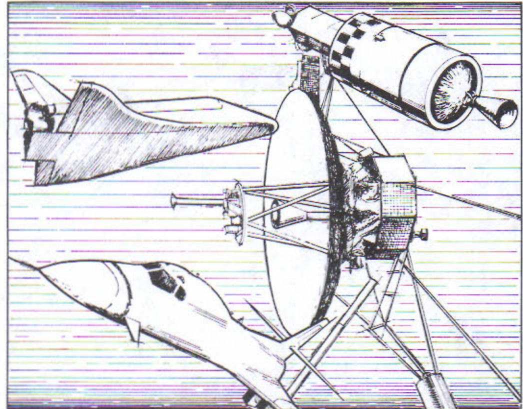
JAN 1N5719 JANTX 1N5719

Features

LARGE DYNAMIC RANGE

LOW HARMONIC DISTORTION

HIGH SERIES ISOLATION



Description/Applications

The JAN Series 1N5719 is a planar passivated silicon PIN diode designed for use in RF switching circuits. These devices are well suited for variable attenuator, AGC, modulator, limiter, and phase shifter applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at $T_{CASE}=25°C$

Operating and Storage Temperature Range .... -65°C to +150°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1 x 10^7 hours.

Reverse Voltage (Working) .... 100 V dc
Reverse Voltage (non-rep) .... 150 V pk
Power Dissipation [At 25°C] .... 250 mW

Derate at 2.0 mW/°C above T_{CASE} = 25°C; assumes an infinite heat sink.

Electrical Specifications at $T_A=25°C$

(Per Table I, Group A Testing of MIL-S-19500/443)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	150		V	$I_R = 10\mu A$
Forward Voltage	V_F		1.0	V	$I_F = 100 mA$
Reverse Current	I_R		250	nA	$V_R = 100V$
Reverse Current	I_R		15	μA	$V_R = 100V, T_A = 150°C$
Capacitance	C_{VR}		.30	pF	$V_R = 100V, f = 1 MHz$
Series Resistance	R_S		1.25	Ω	$I_F = 100 mA, f = 100 MHz$
Effective Carrier Lifetime	τ	100		ns	$I_F = 50 mA, I_R = 250 mA$

JAN 1N5719: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/443.

JANTX 1N5719: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/443. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5719 above.

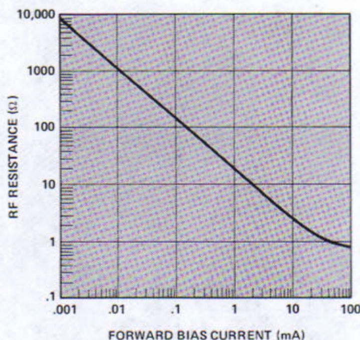
Group B Sample Acceptance Tests**	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051F
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Hermetic Seal	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Salt Atmosphere	1041
Temperature Storage (T_A = 150°C, t = 1k hrs.)	1031
Operating Life (I_o = 70mAdc, V_R = 120V [pk], f = 60Hz, T_A = 25°C, t = 1k hrs.)	1026

Group C Sample Acceptance Tests**	Method MIL-STD-750
Barometric Pressure	1001
Reverse Current	4016
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051F
Low Temperature Operation (−65°C)	
Forward Voltage	4011
Breakdown Voltage	4021
TX Screening (100%)	
High Temp Storage (150°C, 48 hrs.)	1032
Temperature Cycling	1051F
Constant Acceleration	2006
Fine Leak	1071 G or H
Gross Leak	1071E
Burn-in (I_o = 70mAdc, V_R = 120V [pk], T_A = 25°C, f = 60Hz, t = 96 hrs.)	
Evaluation of Drift (I_R, V_F)	

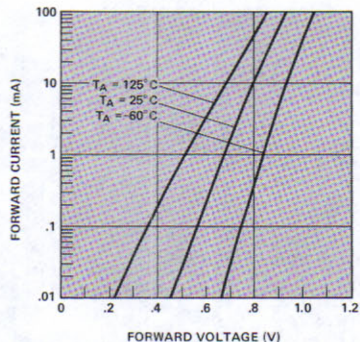
*MIL-STD-202, Method 215

**Subgroup endpoints and measurements per MIL-S-19500/443.

Typical Parameters



Typical RF Resistance vs. Forward Bias Current.



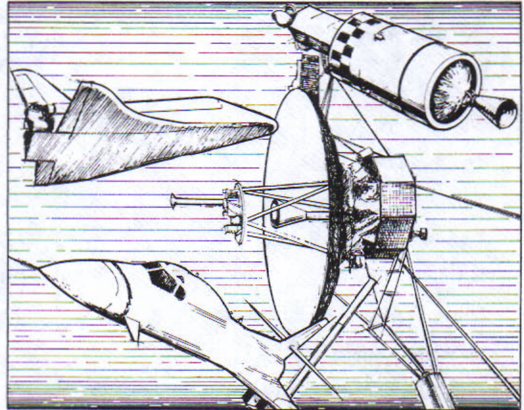
Typical Forward Current vs. Forward Voltage.

High Reliability Products

HEWLETT
PACKARD

STANDARD HIGH RELIABILITY TEST PROGRAMS

Description



In addition to military qualified (JAN/JANTX) Schottky barrier and PIN diodes, Hewlett-Packard offers a line of standard high reliability test programs for some of our commercial devices. These programs are patterned after MIL-S-19500 and are designed to:

1. Eliminate the costly requirement of generating High-Rel specifications, and
2. Offer improved delivery for many High-Rel devices.
3. Aid in writing High-Rel specifications, if required.

Three basic levels of High-Rel testing are offered on our diodes, bipolar transistors, and GaAs FETs.

1. The TX prefix indicates a part that is preconditioned and screened to a program similar to that shown in Table II. (Table V for chips and beam leads)
2. The TXB prefix identifies a part that is preconditioned and screened to TX level with a Group B quality conformance test as shown in Table IV. (Table VI for chips and beam leads)
3. The TXV and TXVB prefix indicates that an internal visual is included as part of the preconditioning and screening.

From these three basic levels, several combinations are available. Please refer to Table I as a guide.

Detailed Specification Sheets are available for all devices in the program. Standard high reliability GaAs FET products are represented following Table VI of this section. Please contact your local HP sales office for additional information.

Table I. Hi-Rel Test Levels. RFQ Information:

Inspection Level	Diode with 5082 Prefix	Diode with HSCH Prefix	Diode with HPND Prefix	Transistor with HXTR Prefix
Commercial	5082-XXXX	HSCH-XXXX	HPND-XXXX	HXTR-XXXX
100% Screen	TXAAAA	TXSAAAA	TXPXXXX	TXTXXXX
100% Screen and Group B	TXBAAAA	TXBSAAAA	TXBPXXXX	TXBTXXXX
100% Screen and Visual	TXVAAAA	TXVSAAAA	TXVPXXXX	TXVTXXXX
100% Screen and Visual and Group B	TXVB3080	TXVBSAAAA	TXVBPXXXX	TXVBTXXXX

Table II. Typical 100% Screening Program for Packaged Devices[1]

Screening Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions[2]
1. Internal Visual Inspection (TXV, TXVB options only)	2074 (Glass Body) 2072 (Other)	
2. High Temperature Life (Non-Operating)	1032	48 Hours Min. at T_{STG} (Max.)
3. Temperature Cycle	MIL-STD-883, Method 1010	10 Cycles, T_{STG} (Min.) to T_{STG} (Max.), 30 Min. per Cycle. Delete para 3.1.
4. Constant Acceleration	2006	20,000G, Y_1 Axis
5. Hermetic Seal, Fine Leak	1071	G or H
6. Hermetic Seal, Gross Leak	1071	A or C, Step 1 Only
7. Burn-In (HTRB)	1038	PIN and SRD only. 48 Hours Min., 80% V_{BR}, $T_C \geq 100°C$
8. Serialization	—	
9. Interim Electrical Test (Delta Parameters)	—	Read and Record — Note [3]
10. Burn-In	1038	96 Hours Min., 25°C
11. Final Electrical Test	—	Same as Step 9.
12. Stability Verification	—	Note [3]
13. Percent Defective Allowable	—	Note [4]
14. Radiographic Inspection (Option, must be specified)	2076	

Table III. Typical Group A Inspection for Packaged Devices[1]. Each Lot is Submitted to Group A Inspection.

Test/Inspection	MIL-STD-750 Method	Conditions	LTPD
Subgroup 1 Visual and Mechanical	2071	—	15
Subgroup 2 DC Electrical Tests at 25°C	—	Note [2]	5
Subgroup 3 Dynamic Electrical Tests at 25°C	—	Note [2]	5

Table IV. Typical Group B Quality Conformance Inspection for Packaged Devices[1]

Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2066	—	15
Subgroup 2 (destructive)			
Solderability	2026	—	15
Resistance to Solvents	1022	Note [5]	
Subgroup 3 (destructive)			
Temperature Cycle	MIL-STD-883, 1010	10 Cycles, T_{STG} (Max.) to T_{STG} (Min.), 30 Min. per Cycle. Delete para 3.1.	10
Thermal Shock	1056	A	
Terminal Strength, Tension	2036	A	
Hermetic Seal, Fine Leak	1071	G or H	
Hermetic Seal, Gross Leak	1071	A or C, Step 1 Only	
Moisture Resistance	1021	Omit Initial Conditioning	
Visual and Mechanical Insp.	2071	—	
Electrical Test	—	Same as Table II Step 9	
Subgroup 4			
Shock	2016	Non-Operating 1500G, 0.5ms, 5 Blows Each X_1, Y_1, Z_1 (Y_1 only for glass body)	10
Vibration, Variable Frequency	2056	—	
Constant Acceleration	2006	20,000G, X_1, Y_1, Z_1,	
Electrical Test	—	Same as Table II, Step 9	
Subgroup 5 (destructive)			
Terminal Strength, Lead Fatigue	2036	E, Note [5]	15
Subgroup 6			
High Temperature Life (Non-Operating)	1032	Same as Table II, Step 2. 340 Hours Min.	5
Electrical Test	—	Same as Table II, Step 9	
Subgroup 7			
Steady State Operation Life	1027	Same as Table II, Step 10. 340 Hours Min.	5
Electrical Test	—	Same as Table II, Step 9	

Table V. Typical 100% Screening Program for Chips and Beam Leads

Screening Test/Inspection	MIL-STD-750 Method	Conditions[2]
1. Electrical Test	—	
2. Visual Inspection	2073 (Chips) HP Spec A5956-0112-72 (Beam Leads)	

Table VI. Typical Group B Lot Acceptance Test for Chips and Beam Leads

Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions[2]	LTPD
1. Assemble Samples in Carrier[6]	—	—	—
2. Electrical Test (Go/No Go)	—	—	100%
3. High Temperature Life (Non-Operating)	1032	48 Hours Min. at T_{STG} (Max.)	100%
4. Temperature Cycle	MIL-STD-883, Method 1010	10 Cycles, T_{STG} (Min.) to T_{STG} (Max.), 30 Min. per Cycle. Delete para 3.1.	100%
5. Burn-In (HTRB)	1038	PIN and SRD Only. 48 Hours Min., 80% V_{BR}, $T_C \geq 100°C$	100%
6. Serialization	—	—	—
7. Interim Electrical Test (Delta Parameters)	—	Read and Record — Note [3]	100%
8a. Burn-In	1038	168 Hours Min., 25°C	10
8b. Final Electrical Test	—	Same as Step 7	
8c. Stability Verification	—	Note [3]	

NOTES:

1. Recommended for devices in the following HP package outlines:
   Glass Body — 11, 15, 12 (delete steps 1, 5, 6 for outline 12).
   Other Coaxial Leaded Bodies — 31, 38, 40, 41, 44, 46, 49, 56, 62, 64, 65
   Stripline/Microstrip Body — C2, C4, E1, H2, H4, 60 (Delete Steps 4-6 for outlines C2, C4, E1)
2. For detailed information on test conditions please request a Hi-Rel specification sheet for the specific product required.
3. Delta Parameters. V_F and C_T are normally chosen for pulse sensitive microwave Schottky diodes. V_F and I_R are normally chosen for PIN, SRD, IMPATT and other Schottky diodes. Δ limits will depend on device type and characteristics.
4. PDA = 15% for pulse sensitive microwave Schottky diodes. PDA = 10% for PIN, SRD and other Schottky diodes.
5. Only applicable for glass body devices.
6. Chips: Outlines 15 (glass body) or 31 (ceramic coaxial lead) Beam Leads: Outline H2 or H4 (stripline).

HEWLETT PACKARD

HIGH RELIABILITY MICROWAVE GaAs FETs

2N6680 TXV
2N6680 TXVB
TXVF-1102
TXVBF-1102

Description

Hewlett-Packard has developed a cost-effective standard test program designed to provide stabilized Gallium Arsenide FETs for applications requiring high-reliability performance. These products are based upon the standard 2N6680 (HFET-1101) and HFET-1102. The preconditioning and screening program for the 2N6680 TXV and the TXVF-1102 is shown in Table I. The 2N6680 TXVB and the TXVBF-1102 are parts which have been preconditioned and screened per Table I and come from a lot which has passed the Group B tests detailed in Table II.

Hewlett-Packard is capable of executing alternative programs based upon individual customer's specifications.

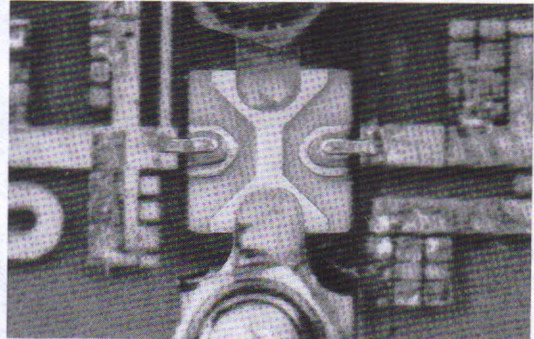
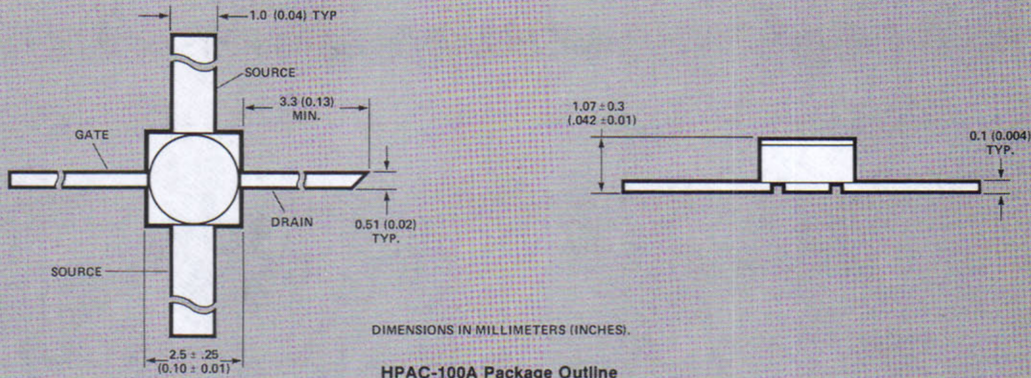


TABLE I
PRECONDITIONING AND SCREENING (100%)

	Examination or Test	MIL-STD-750 Method	Step Conditions
1.	Internal Visual	—	Per HP MSD Procedure A-5956-2150-72
2.	High Temperature Storage	1032	$T_A = 125°C$; $t = 48$ Hours Minimum
3.	Temperature Cycling	1051	Condition B, $T_A = -65°C$ to $+125°C$, Ten (10) Cycles
4.	Constant Acceleration	2006	20,000G, Y_1 Axis
5.	Fine Leak	1071	Condition G or H: 60.0 psig, 4 Hours Soak in He; 5.0×10^{-8} cc-atm/sec.
6.	Gross Leak	1071	Condition A, C or E
7.	Pre Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
8.	Burn-In	1039	Condition B, $T_A = 110°C$, $t = 240$ Hours; $T_{CH} = +125°C$; $V_{DS} = 5.0$Vdc
9.	Post Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
10.	Burn-In Drift Evaluation Calculated from: 72 Hours to 240 Hours		$\Delta I_{DSS} = \pm 15\%$ $\Delta g_m = \pm 15\%$ $\Delta V_{GSP} = \pm 15\%$ $\Delta I_{GSS} = +250$nAdc or $+250\%$, whichever is greater
11.	Percent Defective Calculation		Combining Parameter Limits and Specified Drift, Allow 10.0% Max. Over Burn-in; Resubmit, Permitting Additional 5% if Lot Fails
12.	Group A Testing		
12.1	Visual Examination	2071	a) Marking: Per Data Sheet b) Package Exterior } LTPD = 10
12.2	Electrical Test*		100%. Noise; Gain

*Electrical specifications per HFET-1101/1102 data sheets (Publication numbers 5952-9836 and 5952-9857).



HPAC-100A Package Outline

TABLE II
2N6680 TXV AND TXVBF-1102 GROUP B TESTING PER MIL-S-19500

Examination or Test	MIL-STD-750 Test Method	Environmental Conditions	LTPD
SUBGROUP 1:			20
Physical Dimensions	2066	—	
SUBGROUP 2:			10
Solderability	2026	250° C, Ten (10) sec. Max.	
Thermal Shock	1051	Condition B, Ten (10) Cycles, T_A = -65° C to +125° C	
Hermetic Seal, Fine Leak	1071	Condition G or H, 5x10^{-8} cc-atm/sec., 60 psig, 4 Hrs.	
Hermetic Seal, Gross Leak	1071	Condition A, C or E	
Moisture Resistance	1021	Omit Initial Conditioning	
Endpoints: I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}			
SUBGROUP 3:			10
Mechanical Shock	2016	1500G; 0.5msec; 5 Blows in Each of X_1, Y_1, Y_2 Axis	
Constant Acceleration	2006	20,000G; X_1, Y_1, Y_2	
Vibration Variable Frequency	2056		
Endpoints (per Subgroup 2)			
SUBGROUP 4:			20
Terminal Strength	2036	Condition E, 3.0 ozs. Max.	
SUBGROUP 5:			λ = 15
High Temperature Life	1031	T_A = +125° C	
Endpoints (per Subgroup 2)			
SUBGROUP 6:			λ = 15
Operating Life	1026	T_A = +110° C; T_{CH} = +125° C V_{DS} = +5Vdc	
Endpoints (per Subgroup 2)			

*Electrical specifications per HFET-1101/1102 data sheets (Publication numbers 5952-9836 and 5952-9857).

High Reliability Products

HEWLETT PACKARD

HIGH RELIABILITY MICROWAVE GaAs FETs

TXVF-2201
TXVBF-2201

Description

Hewlett-Packard has developed a cost-effective standard test program designed to provide stabilized Gallium Arsenide FETs for applications requiring high-reliability performance. These products are based upon the standard HFET-2201. The preconditioning and screening program for the TXVF-2201 is shown in Table I. The TXVBF-2201 represents parts which have been preconditioned and screened per Table I and come from a lot which has passed the Group B tests detailed in Table II.

Hewlett-Packard is capable of executing alternative programs based upon individual customer's specifications.

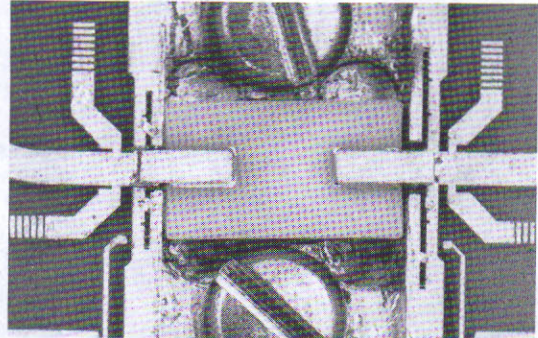
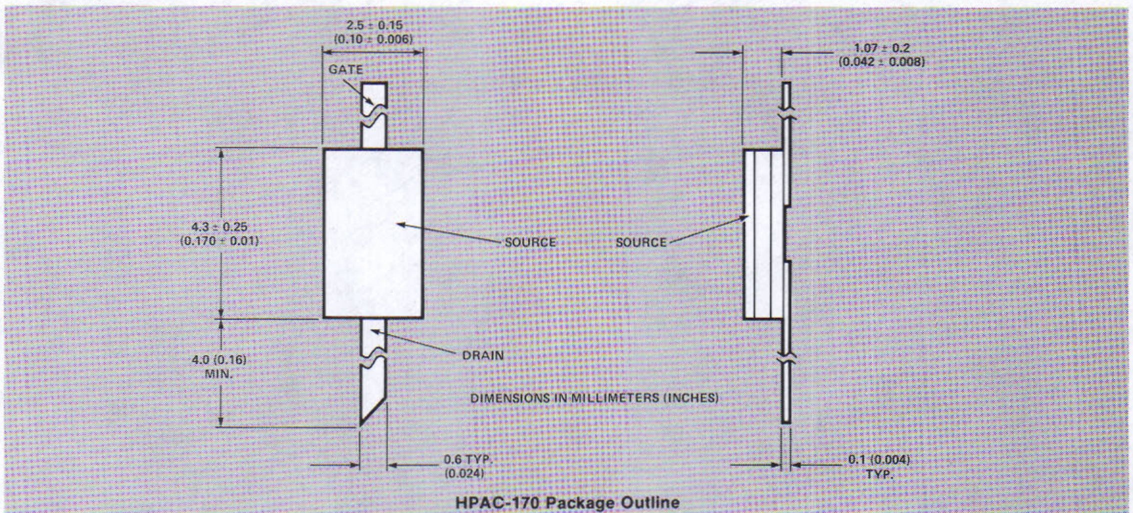


TABLE I
PRECONDITIONING AND SCREENING (100%)

	Examination or Test	MIL-STD-750 Test Method	Step Conditions
1.	Internal Visual	—	Per HP MSD Procedure A-5956-2150-72
2.	High Temperature Storage	1032	$T_A = 125°C$; $t = 48$ Hours Minimum
3.	Temperature Cycling	1051	Condition B, $T_A = -65°C$ to $+125°C$, Ten (10) Cycles
4.	Constant Acceleration	2006	20,000G, Y_1 Axis
5.	Fine Leak	1071	Condition G or H: 60.0 psig, 4 Hours Soak in He; 5×10^{-8} cc-atm/sec
6.	Gross Leak	1071	Condition A, C or E
7.	Pre Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
8.	Burn-In	1039	Condition B, $T_A = 110°C$, $t = 240$ Hours; $T_{CH} = +125°C$; $V_{DS} = 4.0$ Vdc
9.	Post Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
10.	Burn-In Drift Evaluation Calculated from: 72 Hours to 240 Hours		$\Delta I_{DSS} = \pm 15\%$ $\Delta g_m = \pm 15\%$ $\Delta V_{GSP} = \pm 15\%$ $\Delta I_{GSS} = +250$nAdc or $+250\%$, whichever is greater
11.	Percent Defective Calculation		Combining Parameter Limits and Specified Drift, Allow 10.0% Max. Over Burn-in; Resubmit, Permitting Additional 5% if Lot Fails
12.	Group A Testing		
12.1	Visual Examination	2071	a) Marking: Per Data Sheet, b) Package Exterior — LTPD = 10
12.2	Electrical Test*		100%, Noise; Gain

*Electrical specifications per HFET-2201 data sheet (Publication number 5952-9866).



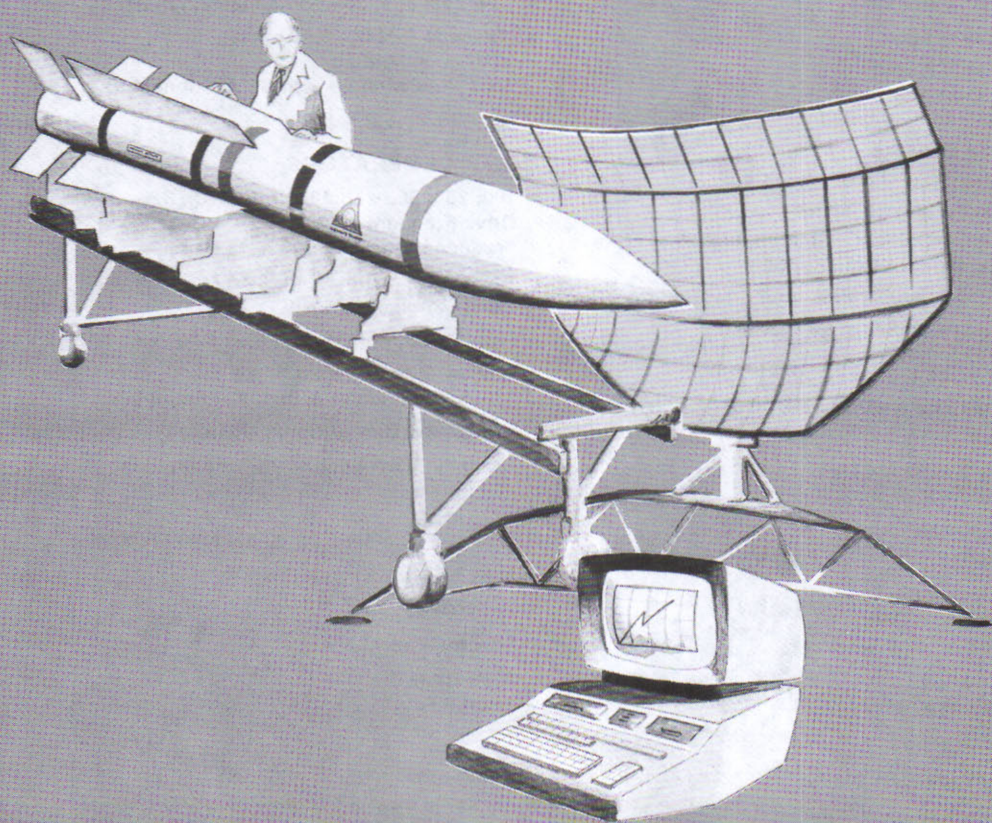
HPAC-170 Package Outline

TABLE II
TXVBF-2201 GROUP B TESTING PER MIL-S-19500

Examination or Test	MIL-STD-750 Test Method	Environmental Conditions	LTPD
SUBGROUP 1:			20
Physical Dimensions	2066	—	
SUBGROUP 2:			10
Solderability	2026	250°C, Ten (10) sec. Max.	
Thermal Shock	1051	Condition B, Ten (10) Cycles, T_A = -65°C to +125°C	
Hermetic Seal, Fine Leak	1071	Condition G or H, 5 x 10^{-8} cc-atm/sec., 60 psig, 4 Hours	
Hermetic Seal, Gross Leak	1071	Condition A, C or E	
Moisture Resistance	1021	Omit Initial Conditioning	
Endpoints: I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}			
SUBGROUP 3:			10
Mechanical Shock	2016	1500G; 0.5msec; 5 Blows in Each of X_1, Y_1, Y_2 Axis	
Constant Acceleration	2006	20,000G; X_1, Y_1, Y_2	
Vibration Variable Frequency	2056		
Endpoints (per Subgroup 2)			
SUBGROUP 4:			20
Terminal Strength	2036	Condition E, 3.0 ozs. Max.	
SUBGROUP 5:**			λ = 15
High Temperature Life	1031	T_A = +125°C	
Endpoints (per Subgroup 2)			
SUBGROUP 6:**			λ = 15
Operating Life	1026	T_A = +110°C; T_{CH} = +125°C V_{DS} = +4.0 Vdc	
Endpoints (per Subgroup 2)			

*Electrical specifications per HFET-2201 data sheet (Publication number 5952-9866).
**Non-destructive

Integrated Products

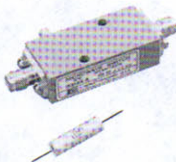


HEWLETT PACKARD

INTEGRATED PRODUCTS

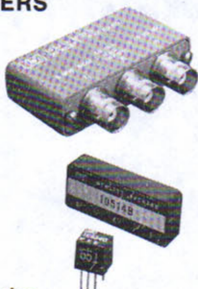
SWITCHES
MODULATORS
LIMITERS
MIXERS
COMB GENERATORS

PIN DIODE SWITCHES



- Broadband, .1-18 GHz
- 33130 Series Optimized for Low Insertion Loss
- 33140 Series Optimized for Fast Swtiching, 5 ns
- Medium and High Isolation Units Available in Each Series
- Hermetic PIN Diode Modules
- Add-On Driver Available for 33140 Series

DOUBLE BALANCED MIXERS

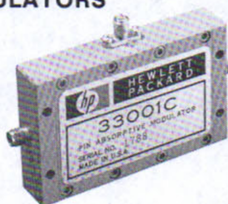


- Broadband
  10534 Series: .05-150 MHz
  10514 Series: .2-500 MHz
- Low Conversion Loss
- Low 1/f Noise, Typically Less than 100 nV per Root Hz
- High Isolation Between Ports
- Wide Range of Package Styles
  "A" Versions: BNC Jacks (Options Available)
  "B" Versions: Pins for PC Mounting
  "C" Versions: Miniature, Pins for PC Mounting
- Hermetically Sealed Schottky Diodes

HMXR-5001 WIDEBAND DOUBLE BALANCED MIXER

- Wideband — 2 to 12.4 GHz Usable to 18 GHz
- Wide IF Bandwidth 0.01 to 1.0 GHz
- Good Conversion Loss
  7.5 dB Typical to 8 GHz
  8.5 dB Typical to 12.4 GHz
- Excellent Isolation
  LO-RF: 30 dB Typical
- Rugged Construction
- Hermetically Packaged Diodes

PIN ABSORPTIVE MODULATORS



- 50Ω Match at all Attenuation Levels
- Greater than Octave Band Coverage
- 50ns Switching (10ns Available on Special Request)
- Hermetic PIN Diode Modules

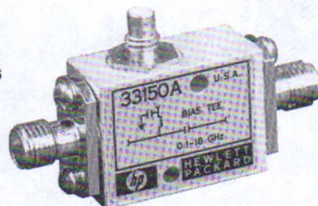
PIN DIODE LIMITERS

- Broadband, .4-12 GHz
- Low Limiting Threshold, 5mW Typical, 8-12 GHz
- Low Insertion Loss, 1.5dB Typical, 8-12 GHz
- Low Leakage, 20mW Typical, 8-12 GHz
- Hermetic PIN Diode Module
  33701A — Module
  33711A — Module with SMA Connectors

COMB GENERATORS

- 100, 250, 500 and 1000 MHz Drive Frequencies (Drive Frequencies in 50-1500 MHz Range Available on Special Request)
- Input Matched to 50Ω
- Self-biased, no External Bias Required
- Narrow Output Pulses:
  130ps Pulse Width with 10V Amplitude
- Broadband Output Comb Up to 40 GHz Available
- Hermetic Step Recovery Diode Modules

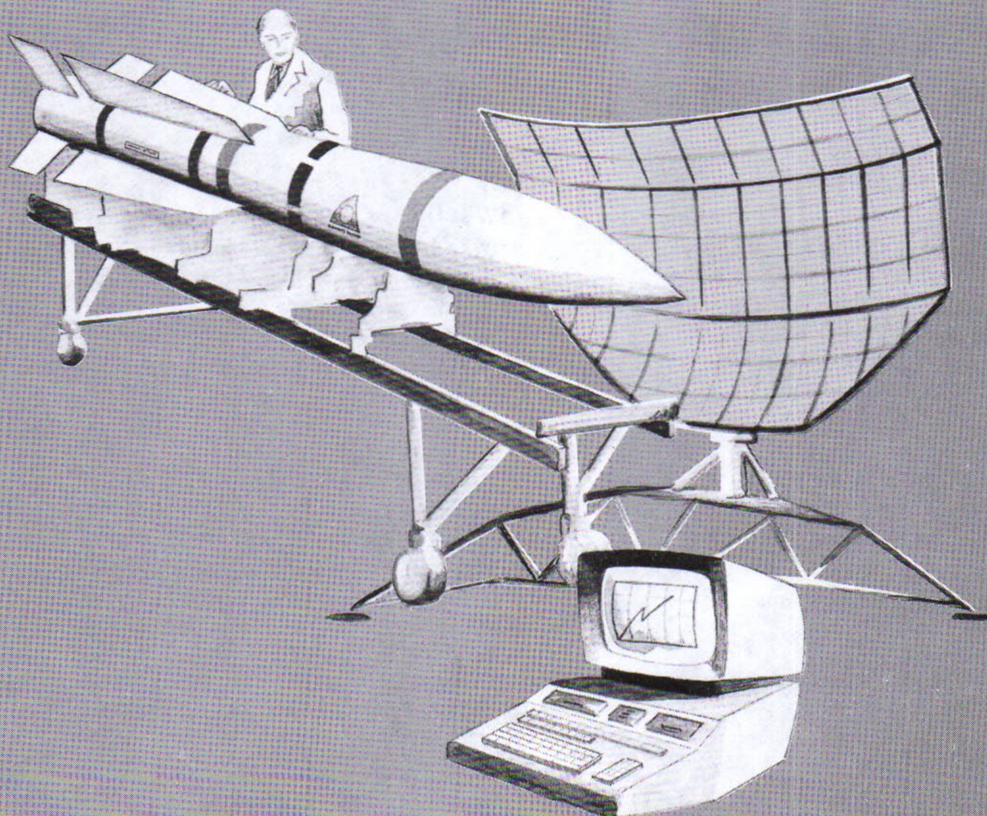
33150A MICROWAVE BIAS NETWORK 0.1-18 GHz



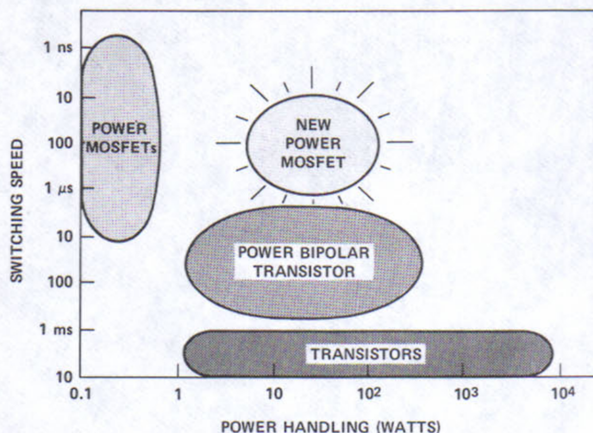
- Wideband
- Low Insertion Loss
- High RF to DC Isolation

For a copy of the new Microwave Integrated Products Catalog (5952-9871D) write: Inquiries Mgr., Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

Power MOS Field Effect Transistors



Power MOSFETs-



Speed Versus Power for Various Power Semiconductor Devices

- **Vertical DMOS**
- **N-Channel**
- **Enhancement Mode**
- **Voltage Controlled**
- **No Storage Time**
- **High Current**
- **High Voltage**
- **Fast Switching**
- **Low ON-Resistance**
- **No Second Breakdown**
- **Ease of Paralleling**
- **Simple Drive Circuits**

High Performance for:

Power Supplies

High breakdown voltage and fast switching speeds with simple drive circuits allow the design of high efficiency circuits for:

- Off-line SMPS
- DC/DC Converters
- Inverters

Motor Controls

High current capability and a broad safe operating area combined with low switching loss are especially useful for:

- Step Motor Drivers
- Chopper Controls
- Synthesized AC

Regulators

High breakdown volage and low switching loss with simple drive circuits are useful for:

- Switching Regulators
- Lamp Ballasts
- High Voltage Linear Regulators

Pulse Circuits

Fast switching speeds with lack of storage time are ideally suited for:

- IMPATT and PIN Diode Drivers
- TWT Modulators
- Pulse Generators

Amplifiers

Wide bandwidth coupled with high power and linear transfer chracteristics are excellent for:

- Class S PWM Amplifiers
- Linear Power Amplifiers
- Class D Ultrasonic Amplifiers

Switching Circuits

Low ON-resistance, voltage control, and high switching speeds are desirable for:

- Solid State Relays
- Analog Switches
- Programmable Power Controls

Hewlett-Packard Power MOSFETs bring high performance to applications which need high voltage, high current and high speed switching transistors.

These devices are manufactured at the Microwave Semiconductor Division, San Jose, California. This facility features advanced wafer fabrication equipment and techniques to include Ion implantation, advanced photo masking systems and computer controlled processing equipment to ensure repeatability and reliability.

For further product details, contact your local HP representative or authorized distributor.

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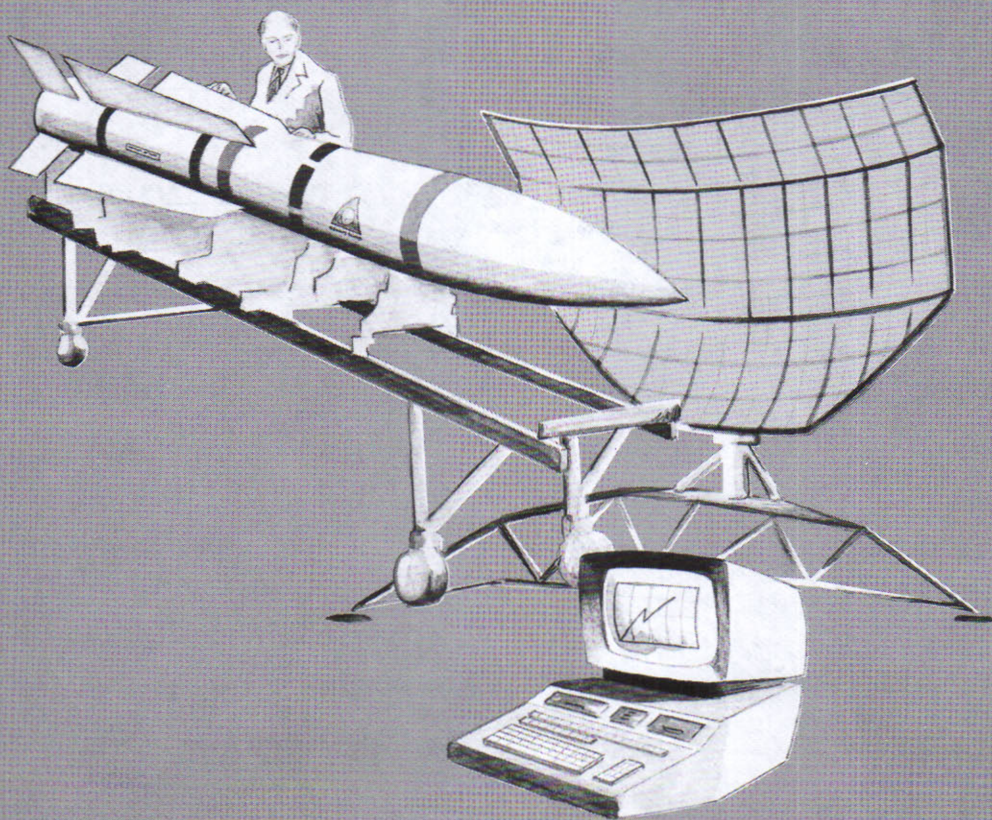

PACKAGE OUTLINES

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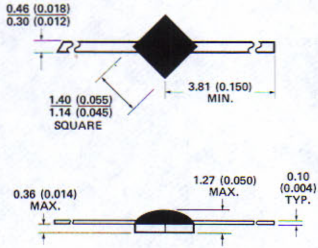
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



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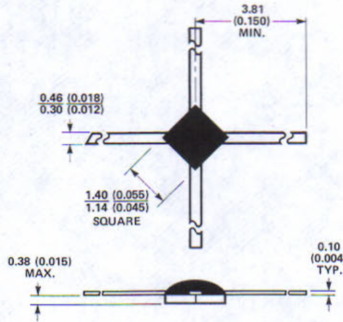

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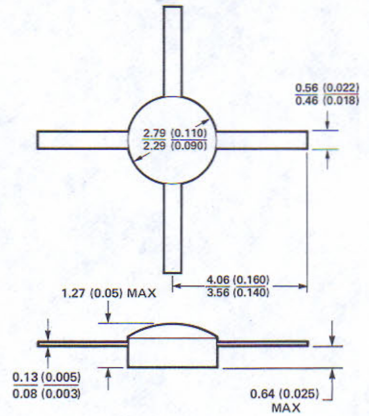

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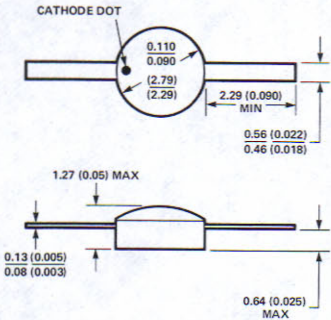

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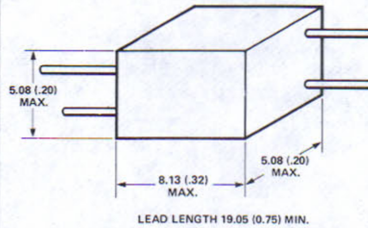

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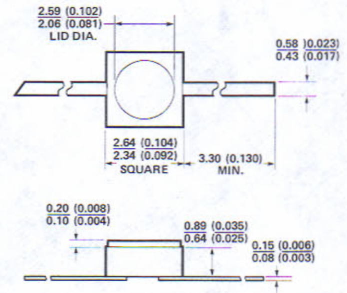

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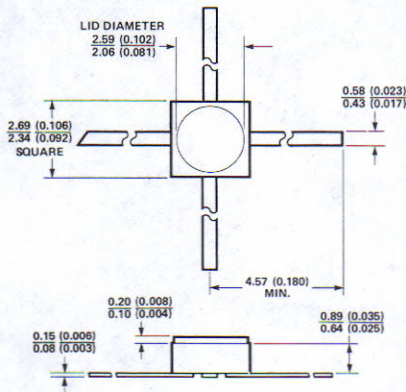

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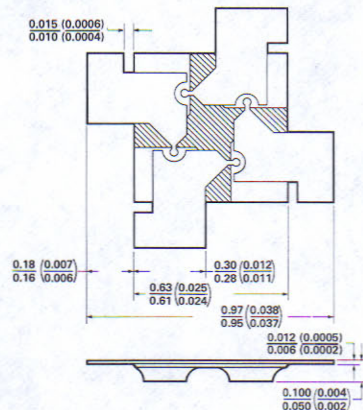

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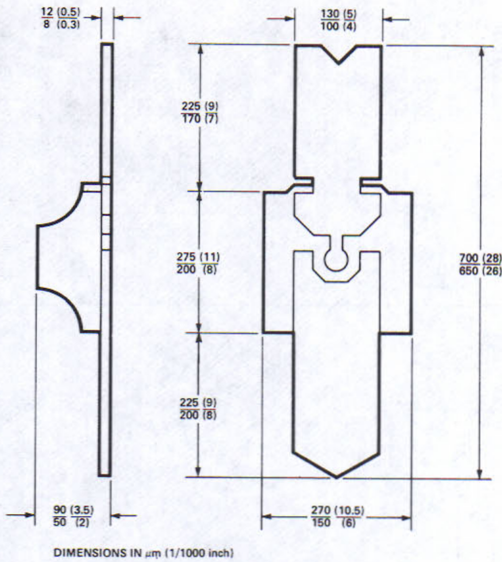

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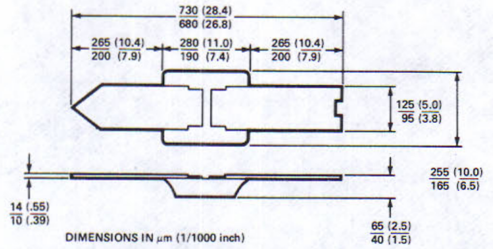

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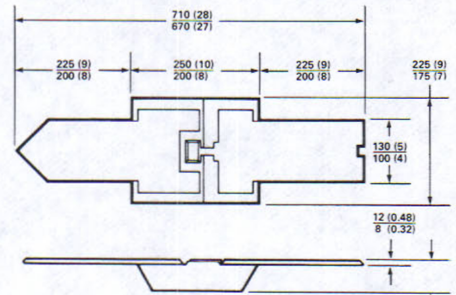

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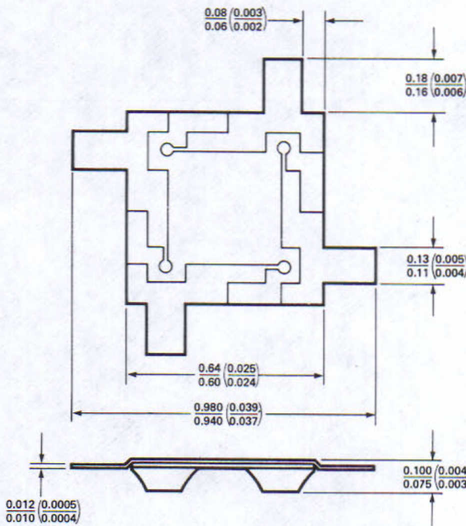

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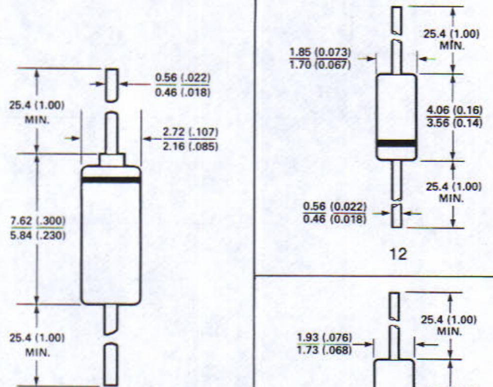

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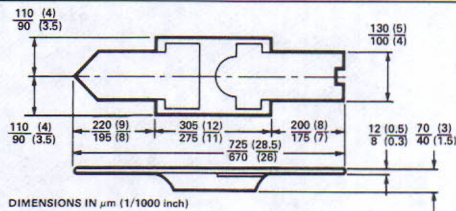

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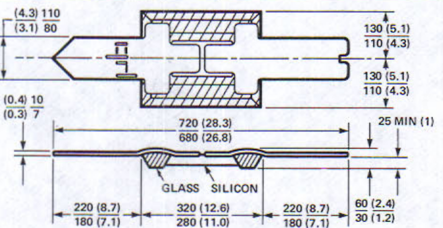

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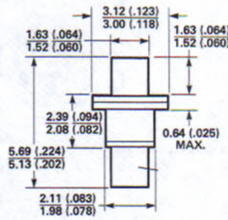

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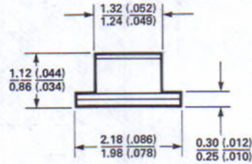

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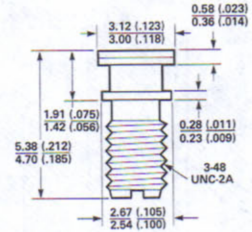

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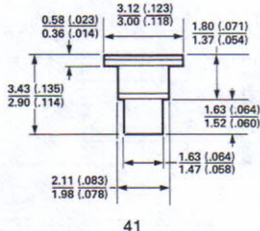

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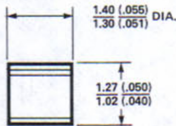

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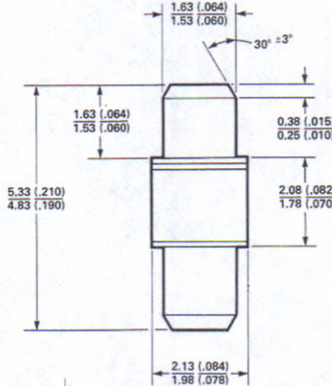

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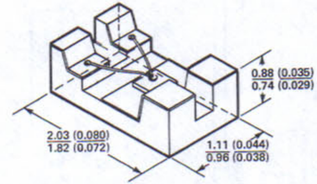

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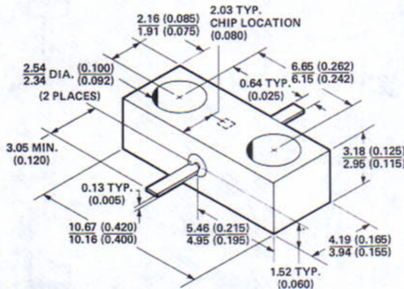

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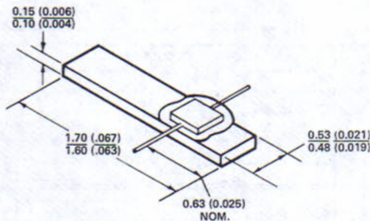

*71 MINISTRIP HAS ONLY ONE LEAD.

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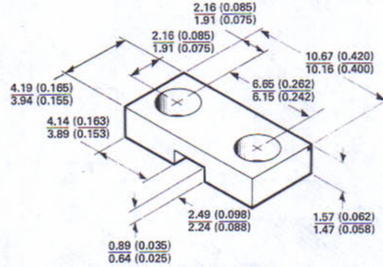

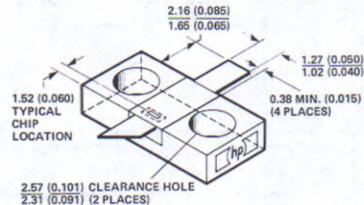

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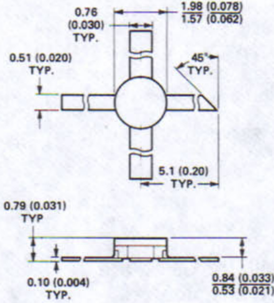

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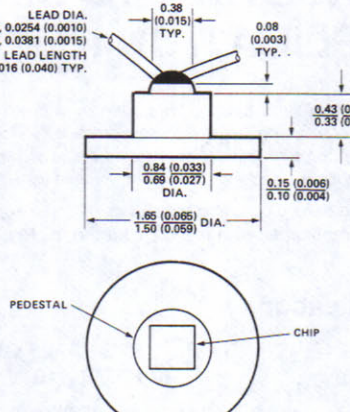

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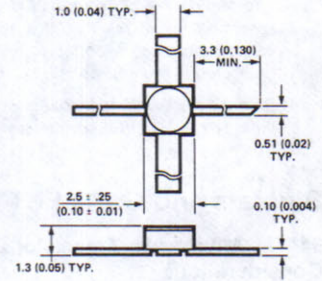

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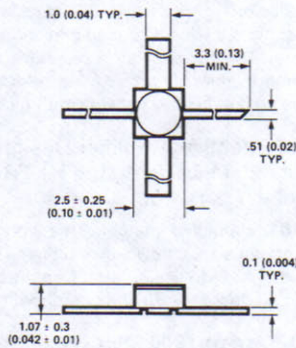

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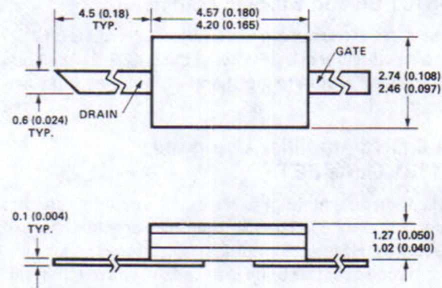

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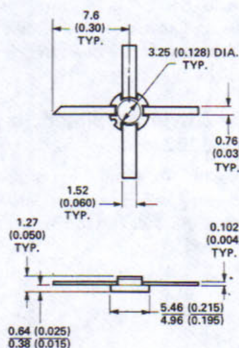

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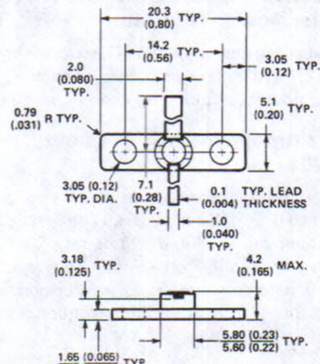

HPAC-200 GB/GT

Appendix

ABSTRACTS OF APPLICATION NOTES

The Microwave Semiconductor Division field sales force is supported by a division applications staff. These technical specialists investigate circuit applications of most interest to the users of these semiconductor devices. The results of these investigations are reported in application notes or in brief application bulletins. Many of these publications have been presented in the appropriate catalog sections in condensed form. A complete list with brief abstracts is presented here.

Below is a brief summary of Application Notes for diodes and transistors. All of the Application Notes are available from your local HP Sales Office or nearest HP Components Authorized Distributor or Representative.

Bipolars and GaAs FET Applications

944-1 Microwave Transistor Bias Considerations

A practical discussion of the temperature dependent variables in a microwave transistor that cause RF performance degradation due to changes in quiescent point. Passive circuit networks that minimize quiescent point drift with temperature are analyzed, and the general equations for dc stability factors are given. Emphasis on practical circuit design is highlighted by typical circuit examples.

967 A Low Noise 4 GHz Amplifier Using the HXTR-6101 Silicon Bipolar Transistor

Describes in detail the design of a single-stage, state-of-the-art, low noise amplifier at 4 GHz using the HXTR-6101 silicon bipolar transistor. Both the input and output matching networks are described.

970 A 6 GHz Amplifier Using the HFET-1101 GaAs FET

This application note highlights some of the design tradeoffs when using a GaAs FET. The example is an amplifier for use in the 5.9 to 6.4 GHz telecommunications band. The amplifier's performance over this band is excellent, with a minimum noise figure of 3.3 dB, a minimum associated gain of 10.9 dB, a flatness of ±0.4 dB and a 9.5 dBm minimum power output at 1 dB gain compression. The maximum input and output SWR are 2.67:1 and 1.90:1 respectively.

972 Two Telecommunications Power Amplifiers for 2 and 4 GHz Using the HXTR-5102 Silicon Bipolar Power Transistor

Describes in detail the design of two linear power amplifiers using the HXTR-5102. In each case, small signal S-parameters and power contours are used in the design.

NEW 973 12 GHz Amplifier Designs Using the HFET-2201

This application note describes in detail two amplifier designs using the HFET-2201 at 12 GHz. The first design is a low noise amplifier on an alumina substrate. The second design is a high gain amplifier on a Teflon fiber glass board. Input and output matching networks are described, and performance over the 11.7 to 12.2 GHz frequency band is plotted.

NEW 975 A 4.3 GHz Oscillator Using the HXTR-4101 Bipolar Transistor

A general technique for transistor oscillator design is illustrated with the details of a 4.3 GHz bipolar oscillator. Small signal S-parameters are used for a preliminary non-oscillating circuit. Measurements of this circuit yield the information needed to complete the circuit design.

NEW 978 The Design of GaAs FET Oscillators

A method of designing microstrip FET oscillators is described. FET oscillators were designed and compared with a bipolar oscillator. The FET oscillators were noisier; however, a substantial improvement in phase noise performance was obtained by using a matching network with higher Q.

NEW 980 A Cost Effective Amplifier Design Approach at 425 MHz Using the HXTR-3101 Silicon Bipolar Transistor

The HXTR-3101, simplified matching networks, and off-the-shelf components are used in an amplifier design which achieves a gain of 13.5 dB at 425 MHz. Construction details include the circuit board layout and component placement.

NEW 981 The Design of a 900 MHz Oscillator with the HXTR-3102

This application note describes two useful techniques for determining the optimum load impedance for an oscillator. The device-line technique applies to an initial circuit, with a negative input resistance at the design frequency, that does not oscillate when loaded by a 50 ohm system, and the load-pull technique applies to an initial circuit that is already oscillating. These techniques are used to design a very efficient 900 MHz oscillator.

NEW 982 A 900 GHz Driver Amplifier Stage Using the HXTR-3102

A modified version of the "load-pull" technique is used in the design of a power driver amplifier stage at 900 MHz. The final output power is 21.5 dBm at 900 MHz. Design and construction details are provided.

Schottky Diode Applications

923 Hot Carrier Diode Video Detectors

Describes the characteristics of HP Schottky barrier diodes intended for use in video detector or video receiver circuits, and discusses some design features of such circuits.

Though less sensitive then the heterodyne receiver, the many advantages of the video receiver make it extremely useful. The Schottky diode can be used to advantage in applications such as beacon, missile-guidance, fuse-activating, and counter-measure receivers, and as power-leveling and signal-monitoring detectors.

Among the subjects discussed are the performance characteristics of video detector diodes — tangential sensitivity, video resistance, voltage sensitivity and figure of merit; how these characteristics affect the bandwidth of a video detector, video detector design considerations; considerations that affect dynamic range; and considerations that vary the level at which burnout can occur.

942 Schottky Diodes for High Volume Low-Cost Applications

Discusses switching, sampling, mixing, and other applications where the substitution of Schottky diodes will provide significant improvement over PN junction devices.

956-1 The Criterion for the Tangential Sensitivity Measurement

Discusses the meaning of Tangential Sensitivity and a recommended measurement technique.

956-3 Flicker Noise in Schottky Diodes

Treats the subject of flicker (1/f) noise in Schottky diodes, comparing 4 different types.

956-4 Schottky Diode Voltage Doubler

Explains how Schottky detectors can be combined to achieve higher output voltages than would be produced by a single diode.

956-5 Dynamic Range Extension of Schottky Detectors

Discusses operation of two types of detectors: the small signal type, also known as square-law detectors; and the large signal type, also known as linear or peak detectors. Techniques for raising the compression level are presented. An example is given illustrating the effect of bias current level on an HP 5082-2751 detector.

956-6 Temperature Dependence of Schottky Detector Voltage Sensitivity

A discussion of the effects that temperature changes have on Schottky barrier diodes. Performance improves at lower temperatures in a predictable manner. Data presented were obtained using HP 5082-2750 detector diodes.

963 Impedance Matching Techniques for Mixers and Detectors

Presents a methodical technique for matching complex loads, such as Schottky diodes, to a transmission line. Direct application to broadband mixers and detectors is illustrated.

969 An Optimum Zero Bias Schottky Detector Diode

Describes the use of the HSCH-3171 and HSCH-3486 zero bias detector diodes. Their forward voltage characteristics are detailed, as well as discussion of voltage sensitivity including effects of junction capacitance, load resistance and reflection loss on sensitivity. Temperature characteristic curves for both devices are also included.

NEW 976 Broadband Microstrip Mixer Design, The Butterfly Mixer

A microstrip mixer on RT/duroid substrate is designed for the frequency range 8 GHz to 12 GHz. Hewlett-Packard Schottky barrier diode model 5082-2207 is used. Low impedance shunt transmission lines are difficult to realize and present a problem in this type of circuit. Radial line stubs are used to avoid this problem.

NEW 986 Square Law and Linear Detection

Frequency, diode capacitance, breakdown voltage, and load resistance all have an effect on the slope of a microwave detector. At high input levels the linearity may be controlled by proper tuning.

NEW 987 Is Bias Current Necessary?

Bias current is often necessary to reduce the impedance of detector diodes to a reasonable level. However, when the signal level is high, rectified current may reduce the impedance without the need for bias current. Measurements with the 5082-2755 diode are used to illustrate this effect.

NEW 988 All Schottky Diodes are Zero Bias Detectors

Diodes which are normally biased make excellent detectors when the bias is eliminated. It is necessary to use a load with an impedance comparable to the diode impedance. This is shown with a 5082-2755 diode used with a 3469B multimeter as the load.

Step Recovery Diode Applications

928 Ku-Band Step Recovery Multipliers

Discusses the use of step-recovery diodes in a times-eight, single-stage frequency multiplier which, at 16 GHz, has a typical maximum output of 75 mW. The note also provides design modifications, together with references, for meeting other performance requirements.

PIN Diode Applications

922 Application of PIN Diodes

Discusses how the PIN diode can be applied to a variety of RF control circuits. Such applications as attenuating, leveling, amplitude and pulse modulating, switching, and phase shifting are discussed in detail. Also examines some of the important properties of the PIN diode and how they affect its application.

929 Fast-Switching PIN Diodes

Discusses the switching speed of the PIN diodes and the considerations which affect switching capability. For HP's 5082-3041/3042 fast switching PIN diodes, AN 929 outlines basic drive requirements and comments on a few practical switching circuits. Considerations involved in the design of the filters required for use with the diodes are also discussed. For the 5082-3041, AN 929 provides two curves: 1) typical isolation vs. forward bias; and 2) switching time vs. forward bias for peak reverse current as a parameter.

932 Selection and Use of Microwave Diode Switches and Limiters

Helps the systems designer select the proper switching or limiting component,and assists him in integrating this component into the overall design of the system. This note is a practical, user-oriented approach to problems encountered with switching and limiting microwave signals.

936 High Performance PIN Attenuator for Low-Cost AGC Applications

PIN diodes offer an economical way of achieving excellent performance in AGC circuits. Significant improvements in crossmodulation and intermodulation distortion performances are obtained, compared to transistors. This note discusses other advantages of PIN diodes, such as low frequency operation, constant impedance levels, and low power consumption.

957-1 Broadbanding the Shunt PIN Diode SPDT Switch

Covers an impedance matching technique which improves the bandwidth of shunt PIN diode switches.

957-2 Reducing the Insertion Loss of a Shunt PIN Diode

Examines a simple filter design which includes the shunt PIN diode capacitance into a low pass filter, thereby extending the upper frequency limit.

957-3 Rectification Effects in PIN Attenuators

Attenuation levels of PIN diodes are changed by high incident power. Variation in attenuation may be minimized by proper choice of bias resistance. Performance of a PIN diode is limited by both carrier level and frequency because of rectification effects. This note presents the effects of frequency, power level, and bias supply for three types of HP diodes: 5082-3170, 3140 and 3141.

971 The Beam Lead Mesa PIN in Shunt Applications

The low RC product, fast switching time, and other unique features of the HPND-4050 beam lead PIN diode make it well suited for switching applications in the shunt configuration. Switching performance, practical circuits, handling, and bonding instructions are included in the discussions in this application note.

985 Achieve High Isolation in Series Applications with the Low Capacitance HPND-4005 Beam Lead PIN

Low capacitance is required for a diode to achieve high isolation in the series configuration. On the other hand, low resistance is needed for low insertion loss. This combination of characteristics in the HPND-4005 Beam Lead PIN diode makes it will suited for series switching applications. The performance of this diode in a SPST switch and a SPDT switch is described in this application note. The equivalent circuits derived in this note would be useful in the design of circuits for switching and other signal control applications.

Hybrid Integrated Circuits Applications

974 Die Attach and Bonding Techniques for Diodes and Transistors

Several package styles are available for use with hybrid integrated circuits. This application note gives detailed instructions for attaching and bonding these devices. A brief description of an impedance matching technique for mixer diodes is also included.

979 The Handling and Bonding of Beam Lead Devices Made Easy

Beam Lead devices are particularly attractive for hybrid circuits because of their low parasitics and small size. The availability of equipment and techniques specifically designed for their small size has facilitated the handling and bonding of these devices. This application note describes some of this equipment and techniques, and outlines suggestions for the proper handling and bonding of Beam Lead devices.

ABSTRACTS OF APPLICATION BULLETINS

Brief summaries of Application Bulletins for diodes and transistors are given here. Portions of many of these have been included in this catalog. All of the Application Bulletins are available from your local HP Sales Office or nearest HP Components Authorized Distributor or Representative.

Transistors

AB 9 Derivation, Definition and Application of Noise Measure

The associated gain at optimum noise figure bias becomes an important parameter at microwave frequencies. The noise measure of a device is a term including both noise figure and associated gain.

AB 10 Transistor Noise Measurements

The increasing acceptance of GaAs field effect and silicon bipolar transistors in low noise pre-amp applications has stressed the importance of the techniques used in measuring noise figure. This application bulletin discusses the various techniques and possible sources of error in making a transistor noise figure measurement.

AB 13 Transistor Speed Up Using Schottky Diodes

Significant reduction in transistor switching delay time can be activated by adding a Schottky diode and a PIN diode to the transistor switching circuit. This improvement in switching performance also extends the oscillator capability of the transistor to higher frequencies.

AB 17 Noise Parameters and Noise Circles for the HXTR-6101, -6102, -6103, -6104 and -6105 Low Noise Transistors

Noise figures as a function of source reflection coefficient (Γ_s) can be expressed using three parameters, F_{min}, R_n and Γ_o known as noise parameters. These parameters are presented for five microwave transistors. The method of generating noise circles is given in a step-by-step fashion.

AB 18 The Performance of the HXTR-6101 at Submilliampere Bias Levels

Describes the performance of a low noise microwave transistor at bias conditions of $V_{CE}=3V$ and $I_C=1.0$ mA, 0.5 mA, 0.25 mA and frequencies 1.0, 1.5, 2.0, and 3.0 GHz.

AB 19 Noise and Power Parameters for the HFET-1101

The noise parameters F_{min}, R_n and Γ_o are given for the HFET-1101, a general purpose microwave GaAs FET. The source and load reflection coefficients are given for maximum output power at an input power level of 5 dBm. The gain, power at 1 dB compression, and power at 3 dB compression are given for frequencies of 4, 6, 8, 10 and 12 GHz.

AB 24 Selecting a Design Medium for the HFET-2201 GaAs Field Effect Transistor

This application bulletin shows measured S-parameters on the HFET-2201 in RT/Duroid and Alumina up to 18 GHz.

AB 37 Details of the HFET-2001 S-Parameter Measurement

This application bulletin presents the test fixture, calibration technique of the fixture, chip placement, and wire bonding scheme used in the S-parameter measurement of the HFET-2001 GaAs FET chip.

Schottky Diodes

AB 5 Current Source for Diode Testing

This application bulletin describes a constant current source designed primarily for the ease of use in laboratory measurements. Easily programmable by thumb wheel switching in 10 μA steps from 10 μA to 700 mA, its accuracy exceeds most commercially available current sources.

AB 7 Mixer Distortion Measurements

Describes the measurement of distortion in a balanced mixer by the two tone method.

AB 13 Transistor Speed Up Using Schottky Diodes

Significant reduction in transistor switching delay time can be achieved by adding a Schottky diode and a PIN diode to the transistor switching circuit. This improvement in switching performance also extends the oscillator capability of the transistor to higher frequencies.

AB 14 Waveform Clipping with Schottky Diodes

Consideration is given in this application bulletin to the design requirements of clipping circuits which are used to limit the transmission of signals above or below specified levels. The characteristics of Schottky diodes needed to achieve the required performance in these circuits are discussed and recommendations made.

AB 15 Waveform Clamping with Schottky Diodes

Discussed in this application bulletin are the circuit design and diode performance requirements for a clamping circuit, which is used as a DC restorer or level shifter. Schottky diodes having the required characteristics for this type of circuit are recommended.

AB 16 Waveform Sampling with Schottky Diodes

This application bulletin discusses the design considerations for a sampling circuit used to sample high frequency repetitive signals and reproduce them at lower frequencies for ease of monitoring. Schottky diode performance requirements important in the realization of a sampling circuit are considered.

AB 26 Using the HSCH-1001 Schottky Diode for Interfacing in Microprocessor Controlled A/D Conversion Circuits

The use of custom codec (coder/decoder) IC chips simplifies the analog to digital circuitry in microprocessor controlled digital switching circuits. This application bulletin describes the use of the HSCH-1001 Schottky diode to achieve the required compatible interface between the codec chip and the rest of the circuit in order to realize optimum circuit performance.

AB 27 Using the HSCH-1001 Schottky Diode in an AGC Detector Circuit

A detector circuit such as one used for AGC or video detection simply realized with the use of the HSCH-1001 Schottky diode is described in this application bulletin.

AB 28 Optocoupler Speedup using the HSCH-1001 Schottky Diode

An optocoupler typically contains a transistor in the output circuit. When the optocoupler is turned on, the transistor is usually in the saturated state, which means the turn-off time will be unnecessarily long. This application bulletin describes how the HSCH-1001 Schottky diode can be used to alleviate the saturation effects on the transistor and thus improve switching time.

AB 30 Using the 5082-2835 Schottky Diode for Protecting and Improving the Performance of an Operational Amplifier

High level voltage spikes degrade the performance of an operational amplifier, and, in extreme cases, destroy the amplifier permanently. This application bulletin describes how the 5082-2835 Schottky diode can be used to protect an operational amplifier against high level voltage overload, and also to improve output response.

AB 31 Using the HSCH-1001 Schottky Diode in a Data Terminal Memory

The simplicity in a read only memory (ROM) circuit allows the circuit to be large in terms of storage capacity. A large capacity requires a large matrix of active devices. The use of HSCH-1001 Schottky diodes in a ROM circuit can ease the power drain because of their low forward voltage. The use of discrete circuit elements offers ease of repair and modification. These and other important considerations are discussed in this application bulletin.

AB 36 Using the HSCH-1001 Schottky Diode in a Digital Logic Gate

Simple "and" and "or" gates consisting of diodes and resistors can be combined into circuits which will perform increasingly complex functions. The achievement of low loss when the diode is biased on and of high isolation when the diode is biased off are the principal characteristics of these types of logic gates. This application bulletin describes how the HSCH-1001 Schottky diode is particularly suited for this type of application because of its low forward voltage and other inherent characteristics.

PIN Diodes

AB 6 PIN Diode RF Resistance Measurment

The use of the HP4815 Vector Impedance Meter, in conjunction with a tunable test fixture, provides an efficient and reliable means for measuring the RF resistance of a PIN diode.

AB 13 Transistor Speed Up Using Schottky Diodes

Significant reduction in transistor switching delay time can be achieved by adding a Schottky diode and a PIN diode to the transistor switching circuit. This improvement in switching performance also extends the oscillator capability of the transistor to higher frequencies.

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Casilla 256-V
SANTIAGO 21
Tel: 225-5044
Telex: 40565 OLYMP CL
C,P

CHINA, People's Republic of
CEIEC Inc.
44 Beiwei Rd.
***BEIJING**, China*
Telex: 22475 CEIEC CN
A,CH,CM,CS,E,P

COLOMBIA
Instrumentación
H. A. Langebaek & Kier S.A.
Apartado Aéreo 6287
***BOGOTÁ** 1, D.E.*
Carrera 7 No. 48-75
***BOGOTA**, 2 D.E.*
Tel: 287-8877
Telex: 44400
Cable: AARIS Bogota
A,CM,E,M,P

COSTA RICA
Cientifica Costarricense S.A.
Avenida 2, Calle 5
San Pedro de Montes de Oca
Apartado 10159
SAN JOSÉ
Tel: 24-38-20, 24-08-19
Telex: 2367 GALGUR
CM,E,M

CYPRUS
Telerexa Ltd.
P.O. Box 4809
14C Stassinos Avenue
NICOSIA
Tel: 62698
Telex: 2894 Levidocy
E,M,P

CZECHOSLOVAKIA
Hewlett-Packard
Obchodni Zastupitelstvi v CSSR
Post. schranka 27
*CS-118 01 **PRAHA 011***
Tel: 66-296
Telex: 121353 IHC

DENMARK
Hewlett-Packard A/S
Datavej 52
DK-3460 **BIRKEROD**
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Telex: 37409 hpas dk
A,CH,CM,CS,E,MS,P

Hewlett-Packard A/S
Navervej 1
DK-8600 **SILKEBORG**
Tel: (06) 82-71-66
Telex: 37409 hpas dk
CH,CM,E

ECUADOR
CYEDE Cia. Ltda.
Avenida Eloy Alfaro 1749
Casilla 6423 CCI
QUITO
Tel: 450-975, 243-052
Telex: 2548 CYEDE ED
A,CM,E,P

Hospitalar S.A.
Robles 625
Casilla 3590
QUITO
Tel: 545-250, 545-122
Telex: 2485 HOSPTL ED
Cable: HOSPITALAR-Quito
M

EGYPT
International Engineering Associates
24 Hussein Hegazi Street
Kasr-el-Aini
CAIRO
Tel: 23-829
Telex: 93830
CH,CS,E,M

Informatic For Systems
22 Talaat Harb Street
CAIRO
Tel: 759006
Telex: 93938 FRANK UN
CH,CS,P

Egyptian International Office
for Foreign Trade
P.O.Box 2558
CAIRO
Tel: 984935
Telex: 93337 EGPOR
P

EL SALVADOR
IPESA de El Salvador S.A.
Boulevard de los Heroes 1148
SAN SALVADOR
Tel: 252787, 259621
Telex: Public Booth 20107
A,CH,CM,CS,E,P

FINLAND
Hewlett-Packard Oy
Revontulentie 7
SF-02100 **ESPOO** 10
Tel: (90) 455-0211
Telex: 121563 hewpa sf
A,CH,CM,CS,E,MS,P

FRANCE

Hewlett-Packard France
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Bureau de Vente de Aix-en-Provence
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F-13090 **AIX-EN-PROVENCE**
Tel: (42) 59-41-02
Telex: 410770F
A,CH,CM,E,MS,P*

Hewlett-Packard France
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F-25026 **BESANCON**
28 Rue de la Republique
F-25000 **BESANCON**
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CH,M

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Bureau de Vente de Lyon
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Boite Postale No. 162
F-69130 **ECULLY** Cédex
Tel: (78) 33-81-25
Telex: 310617F
A,CH,CM,CS,E,MP

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Immeuble France Evry
Tour Lorraine
Boulevard de France
F-91035 **EVRY** Cédex
Tel: (60) 77-96-60
Telex: 692315F
CM,E

Hewlett-Packard France
5th Avenue Raymond Chanas
F-38320 **EYBENS**
Tel: (76) 25-81-41
Telex: 980124 HP GRENOB EYBE
CH,CM

Hewlett-Packard France
Bâtiment Ampère
Rue de la Commune de Paris
Boite Postale 300
F-93153 **LE BLANC MESNIL**
Tel: (01) 865-44-52
Telex: 211032F
CH,CM,CS,E,MS

Hewlett-Packard France
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Avenue du President JF Kennedy
F-33700 **MERIGNAC**
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Telex: 550105F
CH,CM,E,MS

Hewlett-Packard France
32 Rue Lothaire
F-57000 **METZ**
Tel: (87) 65-53-50
CH,CM

Hewlett-Packard France
3 Rue Julien Videment
F-44200 **NANTES**
Tel: (40) 48-09-44
CH**

Hewlett-Packard France
Zone Industrielle de Courtaboeuf
Avenue des Tropiques F-91947 Les Ulis Cédex **ORSAY**
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A,CH,CM,CS,E,MP,P

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F-75782 **PARIS** Cédex 16
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CH,CM,MS,P

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F-35100 **RENNES**
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CH,CM,E,MS,P*

Hewlett-Packard France
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F-76100 **ROUEN**
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A,CH,CM,CS,E,P*

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Bureau de Vente de Lille
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F-59650 **VILLENEUVE D'ASQ**
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Telex: 160124F
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Telex: 4192 TELETRO GU
A,CH,CM,CS,E,M,P

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Telex: 66678 HEWPA HX
Cable: HP ASIA LTD Hong Kong
E,CH,CS,P

Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
HONG KONG
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Telex: 74766 SCHMX HX
A,M

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Elding Trading Company Inc.
Hafnarnvoli-Tryggvagotu
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IS-REYKJAVIK
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M

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Blue Star Ltd.
Band Box House
Prabhadevi
***BOMBAY** 400 025*
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Telex: 011-3751
Cable: BLUESTAR
A,M

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
***BOMBAY** 400 025*
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Telex: 011-4093
Cable: FROSTBLUE
A,CH,CM,CS,E,M

Blue Star Ltd.
Kalyan, 19 Vishwas Colony
*Alkapuri, **BORODA**, 390 005*
Tel: 65235
Cable: BLUE STAR
A

Blue Star Ltd.
7 Hare Street
***CALCUTTA** 700 001*
Tel: 12-01-31
Telex: 021-7655
Cable: BLUESTAR
A,M

Blue Star Ltd.
133 Kodambakkam High Road
***MADRAS** 600 034*
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
A,M

Blue Star Ltd.
Bhandari House, 7th/8th Floors
91 Nehru Place
***NEW DELHI** 110 024*
Tel: 682547
Telex: 031-2463
Cable: BLUESTAR
A,CH,CM,CS,E,M

Blue Star Ltd.
15/16:C Wellesley Rd.
***PUNE** 411 011*
Tel: 22775
Cable: BLUE STAR
A

Blue Star Ltd.
1-1-117/1 Sarojini Devi Road
***SECUNDERABAD** 500 033*
Tel: 70126
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
***TRIVANDRUM** 695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

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BERCA Indonesia P.T.
P.O.Box 496/JKT.
Jl. Abdul Muis 62
JAKARTA
Tel: 373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
Wisma Antara Bldg., 17th floor
JAKARTA
A,CS,E,M

BERCA Indonesia P.T.
P.O. Box 174/SBY.
Jl. Kutei No. 11
SURABAYA
Tel: 68172
Telex: 31146 BERSAL SB
Cable: BERSAL-SURABAYA
A,E,M,P*

Appendix

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Arranged alphabetically by country

IRAQ
Hewlett-Packard Trading S.A.
Mansoor City 9B/3/7
BAGHDAD
Tel: 551-49-73
Telex: 2455 HEPAIRAQ IK
CH,CS

IRELAND
Hewlett-Packard Ireland Ltd.
Kestrel House
Clanwilliam Court
Lower Mount Street
DUBLIN 2, Eire
Tel: 680424, 680426
Telex: 30439
A,CH,CM,CS,E,M,P

Cardiac Services Ltd.
Kilmore Road
Artane
***DUBLIN** 5, Eire*
Tel: (01) 351820
Telex: 30439
M

ISRAEL
Electronics Engineering Division
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3-338973
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
A,CH,CM,CS,E,M,P

ITALY
Hewlett-Packard Italiana S.p.A.
Traversa 99C
Giulio Petrone, 19
I-70124 **BARI**
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/111
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CH,CM,E,MS

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43G/C
I-95126 **CATANIA**
Tel: (095) 37-10-87
Telex: 970291 C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 **CERNUSCO SUL NAVLIGLIO**
Tel: (2) 903691
Telex: 334632
A,CH,CM,CS,E,MP,P

Hewlett-Packard Italiana S.p.A.
Via Nuova san Rocco A
Capodimonte, 62/A
I-80131 **NAPOLI**
Tel: (081) 7413544
A,CH,CM,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 **GENOVA PEGLI**
Tel: (010) 68-37-07 E,C

Hewlett-Packard Italiana S.p.A.
Via Turazza 14
I-35100 **PADOVA**
Tel: (49) 664888
Telex: 430315
A,CH,CM,E,MS

Hewlett-Packard Italiana S.p.A.
Viale C. Pavese 340
I-00144 **ROMA**
Tel: (06) 54831
Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Corso Giovanni Lanza 94
I-10133 **TORINO**
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Telex: 221079
CH,CM,E

JAPAN
Yokogawa-Hewlett-Packard Ltd.
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1-1348-3, Asahi-cho
ATSUGI, Kanagawa 243
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CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Sannomiya-Daiichi Seimei-Bldg. 5F
69 Kyo-machi Chuo-ku
KOBE 650
Tel: (078) 392-4791
C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi Yasoji Bldg 4F
3-4 Chome Tsukuba
KUMAGAYA, Saitama 360
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CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
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1-4-73, San-no-maru
MITO, Ibaragi 310
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CH,CM,E

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Yodogawa-ku
OSAKA, 532
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Telex: YHPOSA 523-3624
A,CH,CM,CS,E,MP,P*

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TOKYO 168
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YOKOHAMA Kanagawa, 221
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CH,CM,E

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Mouasher Cousins Company
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AMMAN
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Telex: 21456 SABCO JO
CH,E,M,P

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City House, Wabera Street
P.O.Box 30635
NAIROBI
Tel: 331955
Telex: 22639
E,M

KOREA
Samsung Electronics
Industrial Products Div.
76-561 Yeoksam-Dong
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SEOUL
Tel: 555-7555, 555-5447
Telex: K27364 SAMSAN
A,CH,CM,CS,E,M,P

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Al-Khalidya Trading & Contracting
P.O. Box 830 Safat
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CH,E,M

Photo & Cine Equipment
P.O. Box 270 Safat
KUWAIT
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Telex: 2247 Matin
P

LEBANON
G.M. Dolmadjian
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BEIRUT
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MP

LUXEMBOURG
Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
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Telex: 23-494 paloben bru
A,CH,CM,CS,E,MP,P

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A,E,M

MALTA
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P

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Tel: 64-2700
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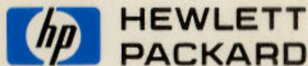
August 1981 5952-6900

Hewlett-Packard Diode and Transistor Designer's Catalog 1982-83



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Printed in U.S.A.
Data Subject to Change
5953-4452 (6/82)